64000

HP64000 Logic Development System

Model 64601A Timing Analysis Control Board

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

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Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

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CW&A 2/81

HEWLETT-PACKARD

SERVICE MANUAL

MODEL 64601A

TIMING ANALYSIS CONTROL BOARD

REPAIR NUMBERS

This Manual applies directly to Models
with Repair Numbers prefixed 2350A.

Manual Part Number 64601-90904
Microfiche Part Number 64601-90804

PRINTED: OCTOBER 1982
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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

SS-1-1 76

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT)

LIST OF ILLUSTRATIONS

LIST OF TABLES

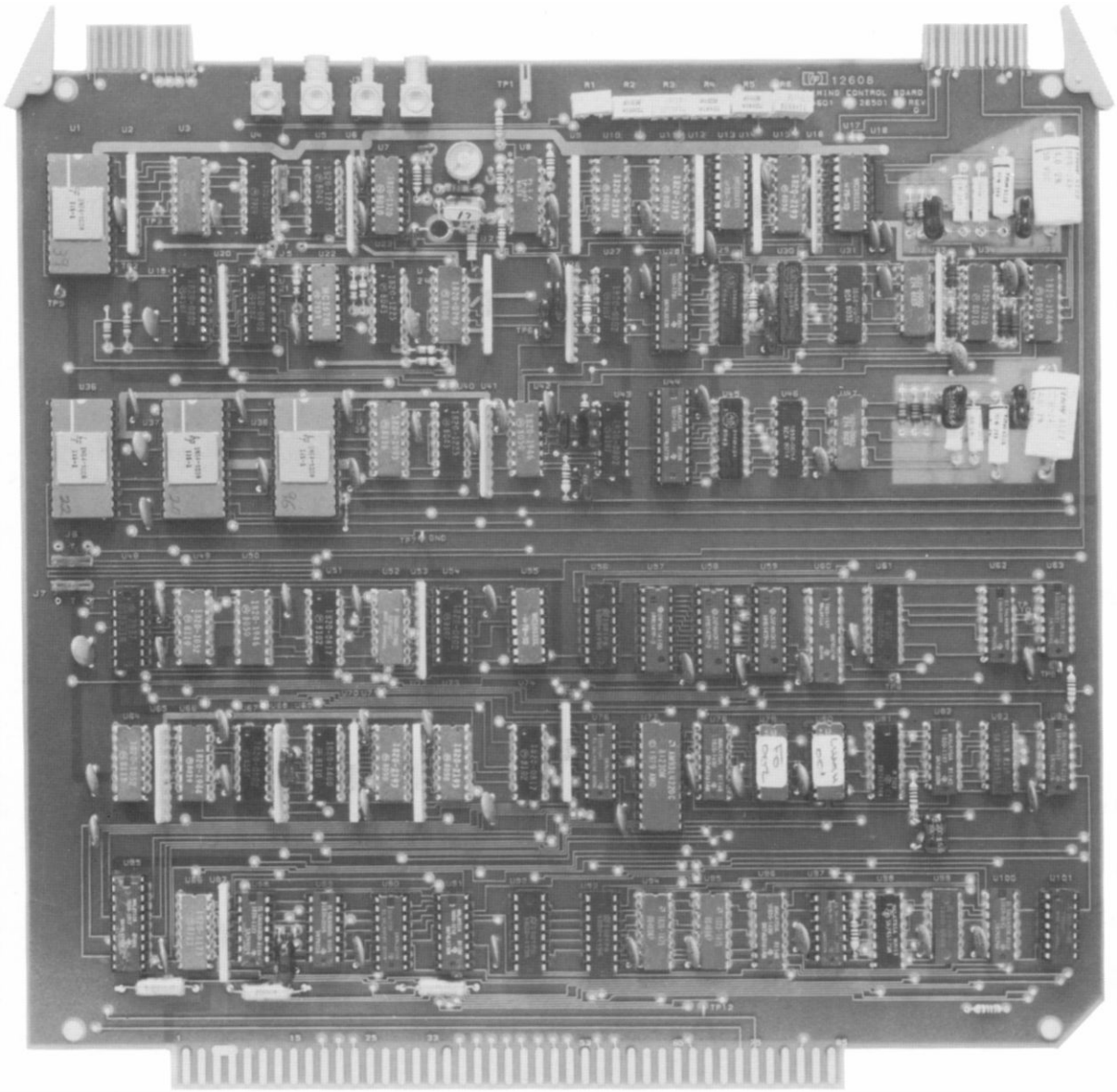

Figure 1-1. Model 64601A Timing Analysis Control Board

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Service Manual contains information required to install, test and service the Hewlett-Packard Model 64601A Timing Analysis Control Board. Operating instructions are provided in a separate Operating Manual supplied with the instrument. It should be kept with the instrument for use by the operator.

1-3. Shown on the title page is a microfiche part number. This number can be used to order 4X6-inch microfilm transparencies of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

1-4. INSTRUMENTS COVERED BY THIS MANUAL.

1-5. Attached to the instrument or printed on the printed circuit board is the repair number. The repair number is in the form: 0000A0000. It is in two parts; the first four digits and the letter are the repair prefix, and the last five are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-6. An instrument manufactured after the printing of this manual may have a repair number prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual for the newer instrument.

1-7. In addition to change information, the supplement contains information for correcting errors in the manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-8. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Office.

1-9. DESCRIPTION.

1-10. The Timing Analyzer is used to monitor information flow in the time domain. The information may be a software program, the actions of a hardware state machine, or random logic signals.

1-11. The Timing Analyzer consists of one Model 64601A Timing Control Board, and from one to two Timing Data Acquisition Boards.

1-12. Up to two Acquisition Boards may be combined to form a Timing Analyzer with as many as 16 channels.

1-13. Logic Analyzers within one Mainframe may be connected together using the Inter Module Bus (IMB). One possible use of the IMB is to allow a State Analyzer to trigger a Timing Analyzer.

1-14. SPECIFICATIONS.

1-15. Instrument specifications are listed in Table 1-1. These specifications are the performance standards or limits against which the instrument is tested.

Table 1-1. Specifications.

Includes Models 64601A Control Board, 64602A 8-Channel Acquisition, and 64604A 8-Channel Timing Probes.

Sample rates
- Wide Sample Mode: variable from 2Hz to 200MHz.
- Glitch mode: variable from 2Hz to 100MHz.
- Dual Threshold: same as Wide Sample Mode.
- Fast Sample: 400MHz.

Memory length:
- Wide Sample, Glitch, & Dual Threshold Modes: 4060 samples.
- 400MHz Mode.....: 8140 samples.

Memory width (8 channel system)
- Wide Sample.....: 8 channels.
- Dual Threshold, Glitch, and 400MHz modes: 4 channels.

Memory width (16 channel system--two acquisition boards)
- Double the width for a single, 8-channel system.

Resolution:
- Total skew from probe tip:
  - Within pod: +/- 1.5ns.
  - Pod to pod: +/- 3.0ns.
  - Conditions: Input signal: VH = -1.0V, VL = -1.6V, VTH at -1.3V
    Input slew rate > .25 V/ns
- Sample rate accuracy: typically +/- .002%

Probe characteristics
- Input Z: 100K ohms +/- 2%, shunted by <6pf.
- Drive requirements:
  - Minimum input amplitude: 600mV P/P.
  - Minimum input overdrive: 200mV or 25% of input amplitude, whichever is greater.
  - Minimum input pulse width: 3.0ns at threshold.
- Dynamic range: +/- 10V.
- Maximum input: +/- 40V.
- Threshold accuracy: +/- 50mV or +/- 2% whichever is greater.
- Hysteresis: Typically 50mV.

Glitch Mode
- Maximum sample rate: 100MHz.
- Minimum width: 3.0ns at threshold.
- Maximum width: sample period less 4.0ns.

Specifications (continued)

Triggering

Time duration accuracy: +/- (20% + 2ns).
Minimum width for narrower-than trigger: 6ns typical.
Minimum width for transition trigger: 6ns typical.
Displayed position accuracy: +/- 4 samples in Wide Sample, Dual Threshold, and Glitch Modes.
: +/- 8 samples in Fast Sample Mode.
Delay from input to external BNC drive: Typically 60ns.
Delay from input to internal IMB drive: Typically 55ns.
Dead time for post-qualify measurement reset.
Typically 50ns + the time required to fill the memory with the selected amount of pre-trigger information.
Reset time for duration trigger: To meet the duration specifications, the trigger duty cycle must be no greater than 40%.

BNC Drive

Output signal swing in transition trigger mode:
Amplitude: 2.0V typical.
Width at 50%: 10ns typical.
Output signal swing in width greater-than trigger mode:
Amplitude: 2.5V typical.
Width: Input trigger width minus the selected duration.
Output signal swing in width less-than trigger mode:
Amplitude: same as in transition trigger mode.
Width: same as in transition trigger mode.
Position: occurs when trigger pattern disappears, before the selected duration times out.

IMB Functions (interconnection with other modules):

Master Enable (LE/ME)-------: drive, receive (Execute/Halt only)
Trigger Enable (LE/TE)------: drive, receive.
Trigger (HE/TR)-------------: drive, receive.
Delay Clock (HE/DCLK)-------: receive only.
Storage Enable (LE/SE)------: not used.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information for installing and removing the Model 64601A. Included are initial inspection procedures, preparation for use, and instructions for repacking the instrument for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. Procedures for checking electrical performance are given in Section IV. If the contents are not complete, if there is mechanical damage or defect, or if the instrument does not pass the Performance Tests, notify the nearest Hewlett-Packard Office. If the shipping container is damaged, or if the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard Office. Keep the shipping materials for carrier's inspection. The HP office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. PREPARATION FOR USE.

2-6. There are no specific preparation for use procedures except the actual installation of the boards in the Mainframe cardcage.

2-7. INSTALLATION INSTRUCTIONS.

WARNING

WHEN REMOVING OR INSTALLING THE TIMING ANALYZER BOARDS, THE MAINFRAME A.C. LINE POWER MUST BE TURNED OFF.

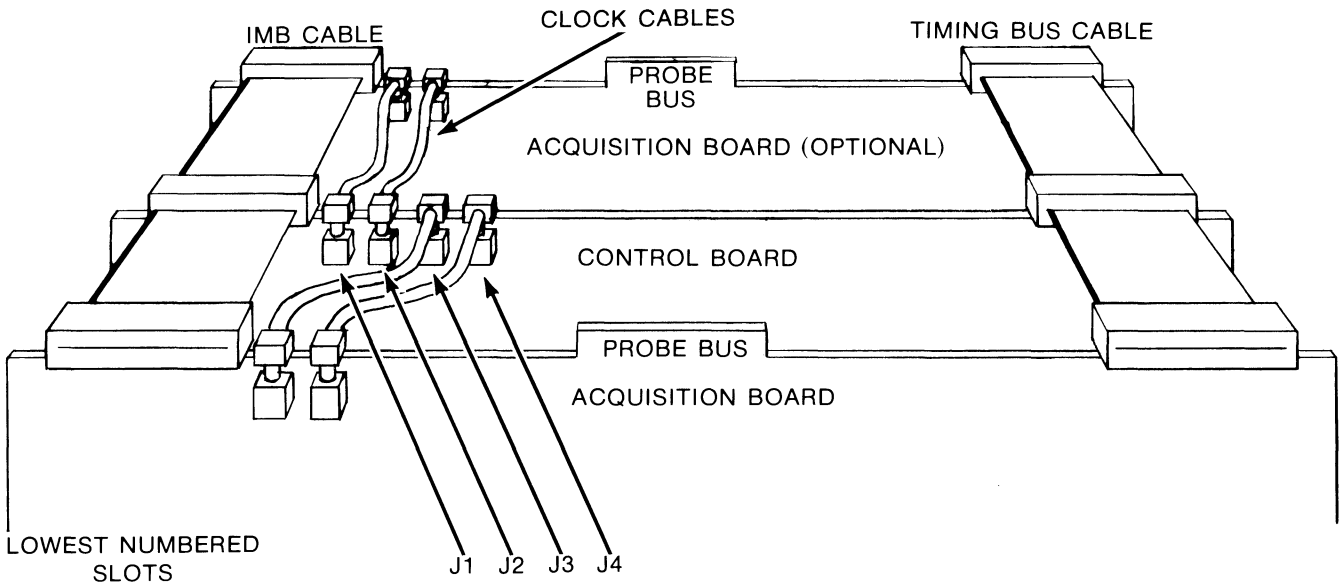

Figure 2-1. Timing Configuration

2-8. Mainframe Configuration.

2-9. Depending on the number of channels required, the timing analyzer will use two or three card slots of the mainframe cardcage.

2-10. One Timing Acquisition Board (64602A) should be installed in the lowest numbered card slot available. The Timing Control Board (64601A) then goes in the next higher slot. And if there is a second Acquisition Board, it will go in the next higher slot. In other words, Acquisition Boards are installed on either side of the Control Board. SEE FIGURE 2-1.

2-11. Up to two Acquisition Boards may be installed with one Control Board forming one Timing Analysis Subsystem.

2-12. Inter Module Bus (IMB).

2-13. Some systems may contain a combination of a timing analyzer and another type of analysis subsystem. The Inter Module Bus, located at the upper left-hand corner of the timing boards (when viewing from the component side) connects two or more analysis modules together for controlling and arming purposes. For example, a Timing Analyzer may arm a State Analyzer, and vice versa.

2-14. The IMB ribbon cable (W3 on the 64601A parts list) is connected the 64601A control board. Although 64602A acquisition boards have an inter module bus jack, there is no electrical connection between this IMB jack and the rest of the board. The 64602A communicates with the IMB through the 64601A control board. Since there is no electrical connection to the 64602A IMB jack and the rest of the board, this jack may have a ribbon cable connected to it for mechanical support.

2-15. Probe Bus

2-16. The timing analyzer communicates with the system under test by means of the 64604A Timing Probe. The probe cable (W2 on the 64602A parts list) connects to the probe bus located on the top center of of the 64602A acquisition board.

2-17. Clock Cables.

2-18. The 64601A control board will supply four sample clock signals to two acquisition boards via SMC jacks J1, J2, J3, and J4 located on the top left-hand part of the board (when viewed from the component side).

2-19. Each 64602A acqusition board requires two clock inputs from the control board. Sample clocks are supplied from the control board to SMC jacks J1 and J2 on the top left-hand part of the acqusition board.

2-20. Clocks should be paired: The left-hand two jacks, J1 and J2, on the control board should be connected to one acquisition board; the right-hand two jacks, J3 and J4 should be connected to a second acquisition board.

2-21. Timing Bus.

2-22. The timing bus is at the top right-hand corner of the 64602A and 64601A timing boards (when viewing from the component side). The timing bus connects the timing Control Board to one or two Acquisition Boards.

2-23. The timing Control and Acquisition Boards must be grouped together to allow the timing bus ribbon cable (W1 on the 64601A parts list) to connect the Control Board to the Acquisition Board. When there are two Acquisition boards, which are placed on either side of the Control Board, a 3-position ribbon cable (W2 on the 64601A parts list) is used. Use only the timing bus cable with the part number given in the 64601A Control Board parts list. The three-position cable (64600-61603) is a special "split" cable which has lines 1-12 cut. See FIGURE 2-2.

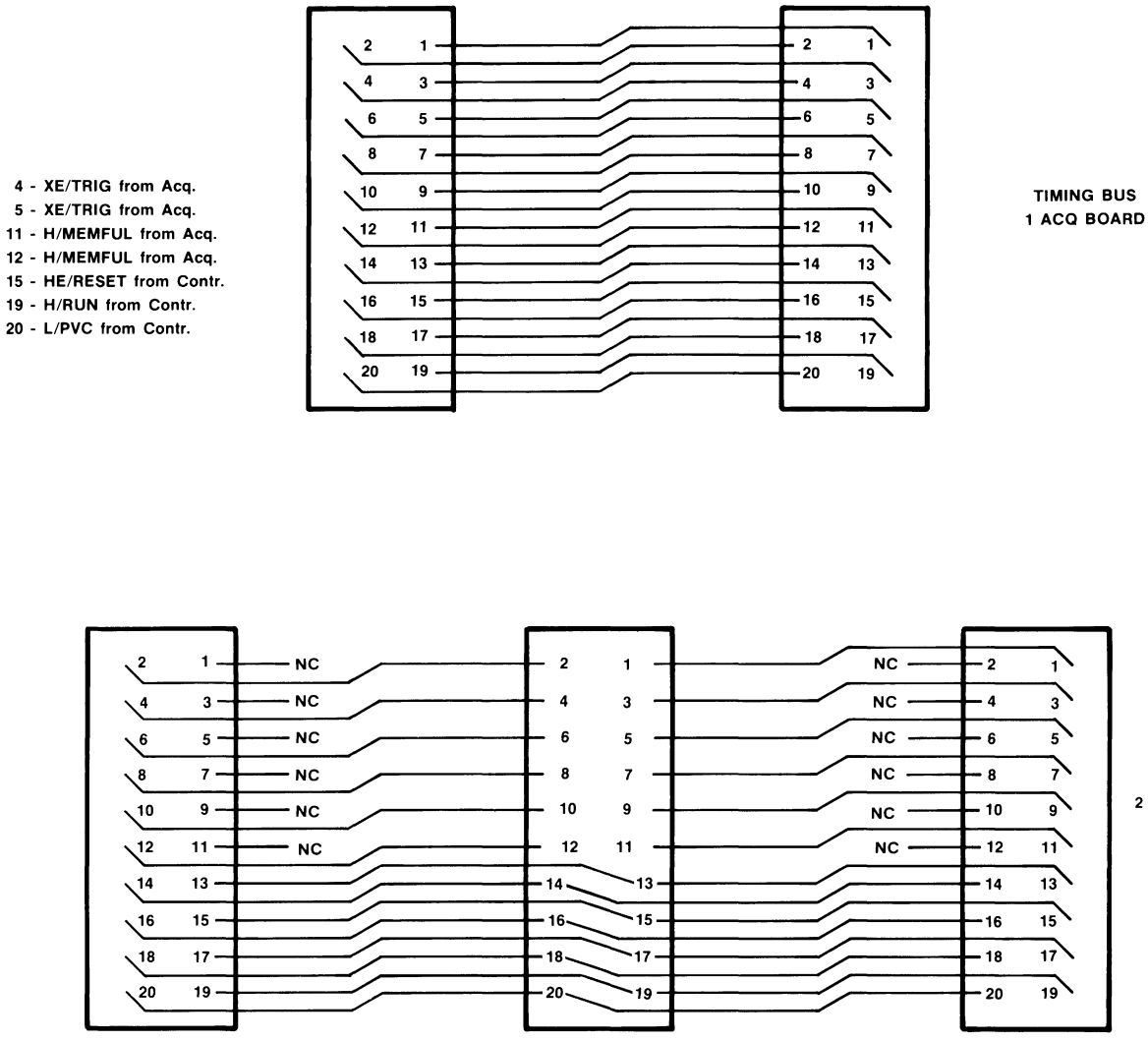

Figure 2-2. Timing Bus Cables

2-24. OPERATING, STORAGE, AND SHIPMENT ENVIRONMENTS.

CAUTION

THE GLITCH (U27) AND ENCODER (U22-25) CHIPS ON THE 64602A ACQUISITION BOARD ARE VERY SENSITIVE TO STATIC. THEY SHOULD BE LEFT IN CONDUCTIVE FOAM UNTIL INSTALLATION. GROUNDING STRAPS AND A GROUNDED WORK STATION ARE RECOMMENDED WHEN HANDLING THE ICS.

2-25. Operating Environment.

2-26. The Model 64601A may be operated in environments within the limits shown below. It should be protected from temperature extremes which cause condensation within the instrument.

Temperature.....+10° to +40° degrees Celsius
Humidity.....5% to 80% relative humidity
Altitude.....4 600 m (15 000 ft)

2-27. Storage Environment.

2-28. The Model 64601A may be stored or shipped in environments within the following limits:

Temperature.....-40° to +70° degrees Celsius
Humidity.....5% to 80% relative humidity
Altitude.....15 000 m (50 000 ft)

2-29. Packing.

2-30. Tagging for Service. If the instrument is to be shipped to a Hewlett-Packard Sales/Service Office for service or repair, attach a tag showing owner (with address), complete instrument repair number, and a description of the service required.

2-31. Original Packing. Containers and materials identical to those used in factory packing are available through Hewlett-Packard Offices. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and complete repair number.

2-32. Other Packing. The following general instructions should be used for repacking with commercially available materials:

a. Wrap instrument in heavy plastic or paper. (If shipping to Hewlett-Packard Office or Service Center, attach a tag indicating type of service required, return address, model number, and complete repair number.

b. Use a strong shipping container. A double wall carton made of 350 pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inches) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and complete repair number.

SECTION III

OPERATION

The operation of the Model 64601A is a function of the system software. Complete system keyboard operation is beyond the scope of the service manual. Please refer to the operator's manual (64601-90903) for the procedure.

NOTES

SECTION IV

PERFORMANCE TESTS

4-1. SECTION IV TABLE OF CONTENTS.

4-2. INTRODUCTION.

4-3. Performance verification tests check the major circuit blocks for proper operation, giving the operator at least 90% confidence that the board is operating correctly.

4-4. There are 15 PV Tests and 3 Supplementary Tests. The supplementary tests use different access instructions. They are described after the the regular 15 PV tests.

4-5. Signature analysis instructions and tables are given at the end of the section.

4-6. The performance verification tests are also used in troubleshooting: (1) They help to isolate troubles to particular blocks, and within particular blocks; (2) Each test corresponds to a one signature loop when running signature analysis.

4-7. Each test is shown on the mainframe screen as a bracket group of 0's. The 0's correspond to steps in a particular test. When the board fails a test step, the "0" for that step becomes a "1".

4-8. TROUBLESHOOTING TECHNIQUES.

4-9. Although each of the PV tests checks a specific circuit block, signals from other blocks are used. A failure in one block can be caused by failures in blocks upstream. When failures occur on a given PV test, check the schematics in TABLE 4-1 below for each test.

Table 4-1. Performance Tests VS Schematic

NUMBER	TEST	CHECK ON SCHEMATIC
1	SERIAL PROGRAMMING	1, 2
2	RUN/HALT/RESET	1, 7
3	TRIGGER	4, 5, 6
4	DELAY COUNTER AND TRIGGER POSITION	7
5	WINDOW	7
6	RATES/INTERVAL (B)	5
7	LESS THAN INTERVAL (B)	5
8	TRANSITION TRIGGER (B)	5
9	DISPLAY DRIVER	8, 9
10	RATES/INTERVAL (A)	4
11	LESS THAN INTERVAL (A)	4
12	TRANSITION TRIGGER (A)	4
13	AND	4, 5, 6
14	OR	4, 5, 6
15	B FOLLOWED BY A	4, 5, 6

4-10. Check board seating.

4-11. Check cable connections.

All cables should be fastened securely. The clock cables should be paired on the left or right two jacks. The timing bus and IMB cables should have the pin 1 wire connected to pin 1 on the jack. No cables other than the two listed in the 64601A Control Board manual parts list may be used for the timing bus.

4-12. Check supply voltages.

Supply voltages from the mainframe (+5V, -5.2V) should be within 5%. The -3.25V should be within 3%.

4-13. Isolate the problem to one board.

When a PV failure occurs, isolate the problem to either an acquisition board, or the control board. Check signatures on the timing bus, which connects the control board to the acquisition board(s). Look first at the signals HE/RUN and HE/RESET from the control board. If these are good, look at the return signals from the acquisition board(s), H/MEMFUL, XE/TRIG1(2). In a two-acquisition board system, H/MEMFUL comes from the acquisition board in the lower numbered slot only.

4-14. Check the programming.

In PV tests the mainframe stimulates the timing analyzer and verifies correct operation by looking at the status registers. Read each test description to see what is being stimulated. Look at the signatures on the outputs of address decoders, data latches, and mode registers where the mainframe is stimulating that PV test circuit block. Correct signatures may be traced back to where signals become incorrect.

4-15. Check the status registers.

A PV failure means the status registers for the control board on service sheet 1 will have one or more incorrect output signatures. The signal path may then be traced back to the problem.

4-16. PHYSICAL SETUP CONDITIONS FOR THE PV TESTS.

4-17. Conditions for the following tests:

a. Connect the timing pod to the 64602A acquisition board by means of timing cable 64604-61601.

b. Leave the probe leads disconnected, so that the probe inputs are floating near ground.

c. Make sure the two clock cables are securely connected. Clock cables should be connected in pairs to either the two right or two left jacks.

d. The timing bus cable should be connected to the jacks at the upper right-hand corner (when viewing from the component side) of both the 64601A control board and the one or two 64602A acquisition board(s). Only timing bus cables (two or three position) listed in the 64601A parts list should be used.

e. NOTE: In noisy environments, ground each probe input, using the ground lead for each probe. Failure to do this may result in the PV displaying intermittent non-existent failures.

4-18. KEYBOARD SETUP (For running all 15 PV tests repeatedly).

4-19. To verify that the entire board is operating correctly, perform the following steps on the mainframe keyboard: (FIGURE 4-1)

a. With the operating system initialized and awaiting a command, press the softkey labeled "opt_test" (you may have to keep pressing the "etc" softkey until you see "opt_test" on the screen). Or you may type "option_test" in lower case.

b. Press [RETURN]. You should see a listing of all the optional boards that are present in your mainframe, along with their slot numbers.

c. Type in the 64601A timing control board slot number. [RETURN]

d. Press softkey "run".

e. Press softkey "slot".

f. Type in the 64601A timing control board slot number.

g. Press softkey "repeated".

h. Press [RETURN]. As shown in Figure 4-1, the screen will now show all 15 Control Board PV tests. Tests that pass will be indicated by "0", and failures will be indicated by "1". The screen will also show the number of times the tests are run, and the number of failures.

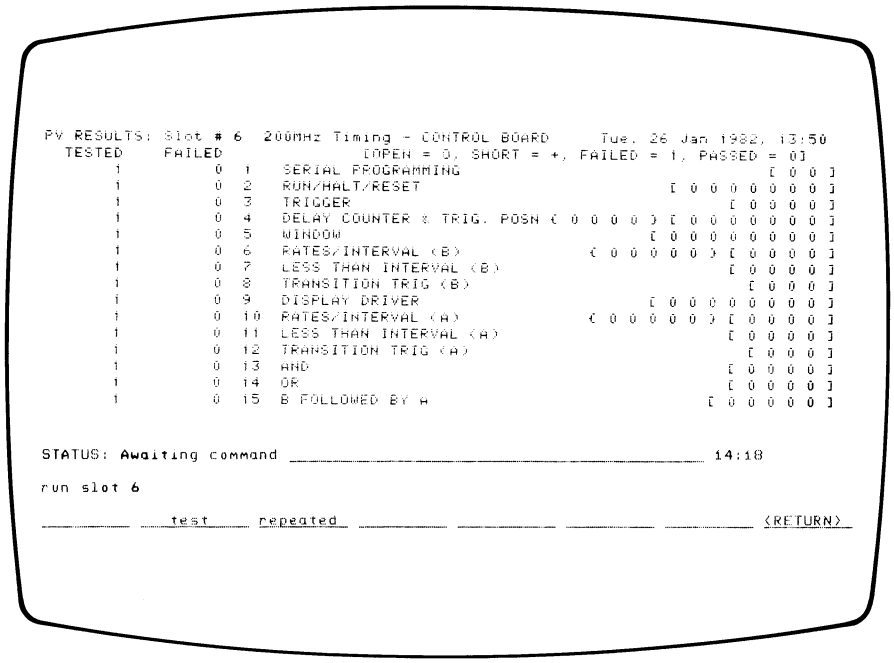

Figure 4-1. PV Test Display (16-channel system).

4-20. KEYBOARD SETUP (For running one PV test repeatedly).

4-21. To run one test at a time repeatedly for signature analysis, perform the following steps: (Figures 4-2 TO 4-10)

a. Press softkey "opt_test". [RETURN]

b. Type in the 64601A timing control board slot number. [RETURN]

c. Press softkey "run".

d. Press softkey "slot".

e. Type in the 64601A timing control board slot number.

f. Press softkey "test".

g. Type in the number of the test you wish to run.

h. Press the soft key "repeated". [RETURN]

4-22. EXPLANATION OF THE TEST DESCRIPTIONS.

4-23. There are 15 (9 in an 8-channel system) performance verification tests for the timing control board. Each of these tests has one or more test steps, denoted by the 0's or 1's within brackets. A "0" in the bracket indicates a PASS for that test step; and a "1" indicates FAIL.

1.	SERIAL PROGRAMMING [00]	
2.	RUN/HALT/RESET [0000000]	
3.	TRIGGER [0000]	
4.	DELAY COUNTER & TRIG. POSN. {0000}[0000000]	
5.	WINDOW [00000000]	
6.	RATES/INTERVAL (B) {00000}[0000]	
7.	LESS THAN INTERVAL (B) [0000]	
8.	TRANSITION TRIGGER (B) [000]	
9.	DISPLAY DRIVER [00000000]	
10.	RATES/INTERVAL (A) {00000}[0000]	*
11.	LESS THAN INTERVAL (A) [0000]	*
12.	TRANSITION TRIGGER (A) [000]	*
13.	AND [0000]	*
14.	OR [0000]	*
15.	B FOLLOWED BY A [00000]	*

* Not used in an 8-channel, single acquisition-board system.

4-24. The numbered test steps described in each PV test correspond, from left to right, to the 0's or 1's within the displayed brackets.

4-25. The numbered test steps describe the commands given by the system software. They do not call for operator intervention.

4-26. TEST 1: SERIAL PROGRAMMING [0 0]

test steps: 1 2

4-27. Purpose.

This test verifies the programming of the 130-bit control register, consisting of U1, U10, U11, U15, U36, U37, U38, U71, and U73. The 130-bit register is the means for programming the timing analyzer.

4-28. Test Steps. (Description of software execution)

1. The 130-bit shift register is loaded with all HIGHs, and a single LOW is walked through. There should be one LOW, and 129 HIGHs coming out the end of the shift register. The last bit, HE/STOP (U36-4), should be LOW.

2. Perform the above test using 129 LOWs and a single HIGH.

4-29. TEST 2: RUN/HALT/RESET [0 0 0 0 0 0 0]

test steps: 1 2 3 4 5 6 7

4-30. Purpose.

This test verifies that the L/RUN bit at U90-6 can be exercised. The L/RUN bit stops the sample clock and disables the 64602A acquistion board memory address counters when it is high.

The test also verifies that the delay counter (U37), the window counter (U38), the trigger position counter (U51,U52), and the acquisition board memory address counters can be reset to 0.

4-31. Test Steps. (description of software execution)

1. HE/RESET is set high; and the H/HALT bit at U90-6 is set high.
2. The H/HALT bit at U90-6 is set low.
3. The U85 status bits, H/STOP, H/TRIG+DLY, H/MEMFUL, H/TC0, H/TC1, and H/TC2 should all be low.
4. Prior to reset, the acquisition-board RAM counters were programmed to FFFFH; the counters should not be 0000H before reset.
5. The RAM counters should be 0000H after reset.

6,7. If there is a second acquisition board, these steps are the same as 4 and 5 above for the second board.

4-32. TEST 3: TRIGGER [0 0 0 0]

test steps: 1 2 3 4

4-33. Purpose.

This test checks the trigger path from the timing bus through the delay counter (U37).

4-34. Conditions set up by the software.

a. The trigger enable counter (U38), the window counter (U36), and the delay counter (U37) are set for zero delay.

b. HE/AND, HE/ATRANSIT, and HE/BTRANSIT are set HIGH, or true.

c. LE/PDUR>A, LE/PDUR>B, LE/ENTRIGA, and LE/ENTRIGB are set HIGH, or false.

d. Pattern duration is set greater than 5ns.

4-35. Test Steps. (Description of software execution)

The first step checks the trigger path from the term selector (U55) through the delay counter.

1. The 130-bit shift register is programmed for HE/PATT high at U55-2. H/TRIG+DLY at the status register (U85-4) should be high.

In the following three steps the trigger path is checked from the trigger selectors (U13 and U17) through the delay counter.

2. The 130-bit shift register is re-programmed so the analyzer itself will generate a trigger when HE/RESET is low. HE/RESET is set high: H/TRIG+DLY should be low.

3. XE/PVTRIG is programmed high true to the trigger selectors, U13 and U17. H/TRIG+DLY should be high at the status register (U85-4).

4. The trigger from each acquisition board can be programmed high true or low true. If XE/TRIG1, from the acquisition board in the lower numbered slot, is high--whether true or false--step 2 above may fail. Step 4 passes when XE/TRIG1 is low.

4-36. TEST 4: DELAY COUNTER & TRIG. POSN.

	{ 0 0 0 0 } [0 0 0 0 0 0 0 0]
test steps:	1 2 3 4 5 6 7 8 9 10 11

4-37. Purpose.

This test checks the delay counter (U37), and the position counter (U51,U52). The tests in braces compare the delay counter against a software timer: The delay counter must "time out" within a 200us window in order to pass. If the tests in braces fail it may mean that the 25MHz system clock in the mainframe, or the 200MHz timing clock, are significantly off in frequency.

4-38. Conditions set up by the software. For this test, the window counter (U36) and the trigger enable counter (U38) are set to zero.

4-39. Test Steps. (Description of software execution)

1. The delay counter is loaded with a 1010... pattern, resulting in a delay of 167.8ms. H/TRIG+DLY should be false at 167.7ms.

2. H/TRIG+DLY should go true sometime during the 200us interval, between 167.7ms and 167.9ms.

3. The delay counter is loaded with a 0101... pattern, resulting in a delay of 55.8ms. H/TRIG+DLY should be false at 55.7ms.

4. A trigger should occur by the end of the 200us interval, before 55.9ms.

In the following bracket steps, the delay counter is checked against the memory address counters on the acquisition board. When the delay counter times out, it starts the window counter, which determines the "window" in memory between tracepoint (H/TRIG+DLY) and the end of aquisition. Since the window counter has been set to zero for this test, it immediately stops (H/STOP) the RAM counters when the delay counter times out.

5. In steps #1 and #2 above, when H/TRIG+DLY goes true during the 200us interval, it starts the window counter. Since the window counter has been set to zero, H/STOP immediately goes true, stopping acquisition and leaving the RAM counters with a certain count. This count is verified.

6. This is similar to step 5: The RAM counters should be correct at the end of the second 200us interval in steps 3 and 4 above.

DELAY COUNTER (continued)

Because the RAM counters have a capacity of only 256, the above steps could pass when the delay counter is actually off by a multiple of 256. To avoid that possibility, the mainframe processor clock is used to clock the delay, window, and position counters.

Since the processor clock is so much slower than the 200MHz timing analyzer sample clock, only the lower 16 bits of the delay counter are loaded with a pattern.

The signature analyzer is gated ON during the following test steps only.

7. The upper 8 bits of the delay counter are loaded with all 0's, and the lower 16 bits with 5555H. H/TRIG+DLY at the status register (U85- 4) should be false one count before the delay counter is supposed to count out.

8. H/TRIG+DLY should be true on the next count.

9. The upper 8 bits of the delay counter are loaded with all 0's, and the lower 16 bits with 2AAAH. H/TRIG+DLY should be false one count before overflow.

10. The trigger should be true on the next count.

11. This step checks the 3-bit trigger position counter. At the end of step 4, H/TC0 should have been HIGH. Then, during step 7, H/TC1 and H/TC2 go HIGH at different times; and finally, all three, H/TC0, H/TC1, and H/TC3, finish in a LOW state at the end of step 7.

4-40. TEST 5: WINDOW COUNTER [0 0 0 0 0 0 0 0]

test steps: 1 2 3 4 5 6 7 8

4-41. Purpose.

This test checks the window counter (U36) and trigger enable counter (U38).

4-42. Theory.

The trigger enable counter, the window counter, and the delay counter are preset by the 130-bit shift register load during RESET.

The trigger enable counter prevents a trigger until old data has been flushed out of the acquisition board glitch chip and encoders. The trigger enable counter also defines the depth of pre-trigger information in memory. Even in the start-trace mode, some pre-trigger information will be displayed.

When the delay counter times out, it emits H/TRIG+DLY, which starts the window counter. When the window counter times out, it emits H/STOP which stops the sample clock and memory address counters, and ends the trace. The count preset into the window counter determines where H/TRIG+DLY will appear in memory. The "window", then, is the post-tracepoint part of memory.

4-43. Test conditions.

Processor-generated clocks are used for this test, and the delay counter is set to zero.

4-44. Test Steps. (Description of software execution)

1. The trigger enable and window counters are loaded to AAH. Clock until one before the trigger enable counter should fire. H/TRIG+DLY at the status register (U85-4) should be false.

2. Clock once more and HE/ENTRIG from the trigger enable counter should go true, causing a trigger at the status register.

3. Clock until one before the window should close. H/STOP should be false out of the window counter.

4. Clock once more and the window should be shut, causing H/STOP at the status register (U85-2) to be true.

5-8. The trigger enable and window counters are loaded to 155H and tested as above.

4-45. TEST 6: RATES/INTERVAL (B)

	{ 0 0 0 0 0 }	[0 0 0 0]
test steps:	1 2 3 4 5	6 7 8 9

4-46. Purpose.

A user of the timing analyzer may specify pattern durations: a trigger will then occur only when the pattern lasts a given length of time.

In this test a trigger must not occur when the pattern lasts less than the given time. The user may thus ensure that triggering does not occur on transients or shorter patterns.

This test checks the B term generator duration circuits (U44,U46,U47) and the sample rate clock. For a given sample rate, the acquisition board memory address counters are used to verify the accuracy of the selected interval within 20%.

The tests in braces check each capacitor and current source at a different sample rate.

With ranges <1us, the resolution is not good enough to verify the specs.

4-47. Theory.

When tracepoint (H/TRIG+DLY) is generated, the window counter (U36) counts down to determine the amount of "window" between tracepoint in memory and the end of new acquisition. When the window counter times out, it generates H/STOP, stopping the sample clock and, consequently, the acquisition-board RAM counter.

By setting the window counter (U36), the delay counter (U37), and the trigger enable counter (U38) to zero, the only delay between the acquisition-board trigger (XE/TRIG) and H/STOP is that selected by the duration circuits in the term generators.

RATES/INTERVAL B (continued)

4-48. Test Steps. (Description of software execution)

The acquisition board memory address counters verify within 20% the accuracy of the duration circuits. After each test step, the counters are checked. For the duration ciruits to pass, the counters must fall within the allowable range.

1. Duration circuits are set to 10us, sample rate is 50MHz.
2. Duration is set to 100us, sample rate is 200MHz.
3. Duration is set to 1us, sample rate is 100MHz.
4. Duration is set to 50us, sample rate is 40MHz.
5. Duration is set to 200us, sample rate is 10MHz.

The following steps in brackets use a single capacitor and different current sources. If these steps pass, and the previous ones fail, the problem is likely to be a capacitor or the particular sample rate circuitry associated with the step that fails.

6. Duration is set to 2us, sample rate is 200MHz.
7. Duration is set to 5us, sample rate is 200MHz.
8. Duration is set to 10us, sample rate is 200MHz.
9. The last test verifies that HTRIG+DLY was true, or HIGH, in all previous test steps.

4-49. TEST 7: LESS THAN INTERVAL (B) [0 0 0 0]

test steps: 1 2 3 4

4-50. Purpose.

In this test the duration circuits must "time out" before the trigger pattern ends. If "timeout" occurs before the Acquisition Board trigger signal XE/TRIG disappears, the analyzer should trigger.

4-51. Theory.

The B term generator duration circuits ramp down from ground after receiving a LOW trigger signal from U35-14. The mainframe processor programs the time it takes to fire the schmitt circuit (U34).

4-52. Conditions.

a. The acquisition board DACs are set for an "always trigger" condition lasting a specified time.

b. The delay counter (U37) and the trigger enable counter (U38) are set to zero.

c. LE/PDUR>B is programmed true, or LOW; and HE/BTRANSIT false, or LOW. (In other words, we specify level triggering and require the duration circuits to time out while the pattern is still true).

4-53. Test Steps. (Description of software execution)

1. H/TRIG+DLY is initialized false, or LOW.

2. The duration circuits are programmed for a 200us duration. The DAC thresholds are set to cause an "always trigger" for longer than 200us. H/TRIG+DLY should be true at the status register (U85-4).

3. H/TRIG+DLY is initialized false.

4. With the duration circuits still set for 200us, the DACs are programmed to cause an acquisition board trigger signal lasting less than 200us. H/TRIG+DLY should be false.

4-54. TEST 8: TRANSITION TRIGGER (B) [0 0 0]

test steps: 1 2 3

4-55. Purpose.

This test checks the B term generator transition circuits (U42 and U43). Thresholds which simulate a particular pattern are programmed into the acquisition board DACs, and the glitch chip (U27 on the acquisition board) is programmed to trigger on that pattern.

4-56. Theory.

The B term generator transition circuit will cause a trigger on a transition away from, or leaving the specified pattern when HE/BTRANSIT is true and LE/PDUR>B is false.

Under the same conditions, the analyzer will trigger on a transition into, or entering the pattern when the acquisition board trigger XE/TRIG is low true. (The "X" in the mnemonic indicates this signal can be programmed either low true or high true).

4-57. Test Conditions.

a. The delay counter (U37), trigger enable counter (U38), and window counter (U36) are set to zero.

b. HE/BTRANSIT is high. We want to trigger on a transition.

c. LE/PDUR>B is high. We are triggering on a transition, not an interval.

d. XE/TRIG1 from the acq board is programmed low true for this test.

4-58. Test Steps. (Description of software execution)

1. During RESET, the transition circuits are programmed for transition triggering, the DAC thresholds are set up to simulate a pattern, and the glitch chip is programmed to recognize that pattern. During RUN, H/TRIG+DLY should be false because there has been no transition.

2. The pattern on the input is changed. This is a "leaving" transition. H/TRIG+DLY should remain false because XE/TRIG1 is low true.

3. Setting the thresholds back to their original value is, in effect, an "entering" transition. H/TRIG+DLY should go true.

4-59. TEST 9: DISPLAY DRIVER

[0 0 0 0 0 0 0 0]

test steps: 1 2 3 4 5 6 7 8

The Display RAMs are loaded with eight different patterns and read out. This tests the programming, the mode control circuits, the address latches, and the RAMs.

4-60. TEST 10: RATES/INTERVAL (A) (16 CH. ONLY)

	{ 0 0 0 0 0 }	[0 0 0 0]
test steps:	1 2 3 4 5	6 7 8 9

This is the same as TEST 6 above for the B term generator.

4-61. TEST 11: LESS THAN INTERVAL (A) (16 Ch. Only)

	[0 0 0 0]
test steps:	1 2 3 4

This is the same as TEST 7 above for the B term generator.

4-62. TEST 12: TRANSITION TRIGGER (A) (16 Ch. Only)

	[0 0 0]
test steps:	1 2 3

This is the same as TEST 8 for the B term generator.

4-63. TEST 13: AND (16 Ch. Only) [0 0 0 0]

test steps: 1 2 3 4

4-64. Purpose.

This test checks the AND/OR combination circuits (U13,U17,U34,U35). HE/AND is set high.

4-65. Theory.

In a 16-channel, two-acquisition board system, each acquisition board provides a trigger signal to the control board via the timing bus.

These two triggers, XE/TRIG1 and XE/TRIG2 from pods 1 and 2, are ANDed or ORed in the combination circuits.

When the two triggers are both high, and HE/AND is high, they are ANDed. When the one or both of the triggers are low, and HE/AND is low, they are ORed.

XE/TRIG1 and XE/TRIG2 may be programmed as either high true or low true by XE/TRIGPOL out of the glitch chip (U27 on the acquisition board). Hence the "X" designation.

4-66. Test Steps. (Description of software execution)

1. With HE/AND high, XE/TRIG1 and XE/TRIG2 into U13 and U17 are both set low. H/TRIG+DLY should be false, or low at U85-4.

2. Low XE/TRIG1 and high XE/TRIG2. H/TRIG+DLY should be low.

3. High XE/TRIG1 and low XE/TRIG2. H/TRIG+DLY should be low.

4. High XE/TRIG1 and high XE/TRIG2. H/TRIG+DLY should be high.

4-67. TEST 14: OR (16 Ch. Only) [0 0 0 0]

test steps: 1 2 3 4

4-68. Purpose.

This is the same as the above test, execpt that H/EAND is false, or low.

4-69. Test Steps. (Description of software execution)

1. Low XE/TRIG1 and low XE/TRIG2. H/TRIG+DLY should be low at U85-4.
2. Low XE/TRIG1 and high XE/TRIG2. H/TRIG+DLY should be true, or high.
3. High XE/TRIG1 and low XE/TRIG2. H/TRIG+DLY should be high.
4. High XE/TRIG1 and high XE/TRIG2. H/TRIG+DLY should be high.

4-70. TEST 15: B FOLLOWED BY A (16 Ch. Only)

	[0 0 0 0 0]
test steps:	1 2 3 4 5

4-71. Purpose.

This tests the programming, the term generators, the B latching circuit (U67,74), and the arming circuits (U54,55,69).

4-72. Theory.

The A and B term generators select and combine acquisition board triggers. Besides AND/OR combinations, there is a B-before-A combination. A signal satisfying the B term generator is latched, and the analyzer then waits for an A signal to occur before triggering.

LE/ENLATCHB into U55 must be low for the latched B mode.

4-73. Test Steps. (Description of software execution)

1. HE/TRIGA out of the A term generator is high, and HE/TRIGB is low. H/TRIG+DLY should be low at U85-4.

2. Both HE/TRIGA and HE/TRIGB are low. H/TRIG+DLY should be low.

3. HE/TRIGA is low and HE/TRIGB is high: The B latch is now set. H/TRIG+DLY should still be low.

4. Both HE/TRIGA and HE/TRIGB are low. H/TRIG+DLY should be low. The B latch should remain set because there has been no RESET.

5. HE/TRIGA is high and HE/TRIGB is low. We now have an A trigger occurring after a latched B trigger. H/TRIG+DLY should be high.

4-74. SUPPLEMENTARY DISPLAY TEST.

Further confirmation of proper display driver operation may be be obtained visually by pressing the following softkeys in sequence: "run slot __ display_test". Press [RETURN] and the first pattern appears. This pattern verifies, by corner brackets, proper timing display centering. You may observe other test patterns by continuing to press [RETURN] until the first pattern finally reappears.

Fifteen unique patterns are illustrated in figures 4-2 to 4-16. The last 11 patterns (figures 4-5 to 4-16) are repeated eight times in the displays, and shifted by one dot in each display. The repetitions are not shown in the manual.

Except for the eight-dot shift in the patterns following those shown in figures 4-5 to 4-16, the screen patterns should look similar to the illustrations. Intensity alternations cannot be shown in the manual, but will be described.

Although the purpose of the patterns is primarily to generate signatures, defects in the displays may help to isolate problems. For example, address line shorts may put one character adjacent to another. An open line might take away a character that should be there. Or perhaps one character will be substituted for another, eg glitch for cursor. Look primarily for irregularities and discontinuities.

Examples of possible problems:

Irregularities.
Misshapen characters.
Glitch instead of normal data, or vice versa.
Adjacent line shorts may show up as adjacent graticules, cursors, etc.
Blanks instead of characters.
Highs instead of lows, or vice versa.
Transition characters subsituted for other data characters, or vice versa.

Figure 4-2.

This display checks the proper centering of the pattern.

The bar at the bottom and the brackets are generated by the mainframe. The timing analyzer display driver puts out the dot pattern, which should be centered within the brackets as shown.

Problems might be in the Start-Address Latches (U92, 93) or the Row, Char, or Line Counters (U78, 94-96).

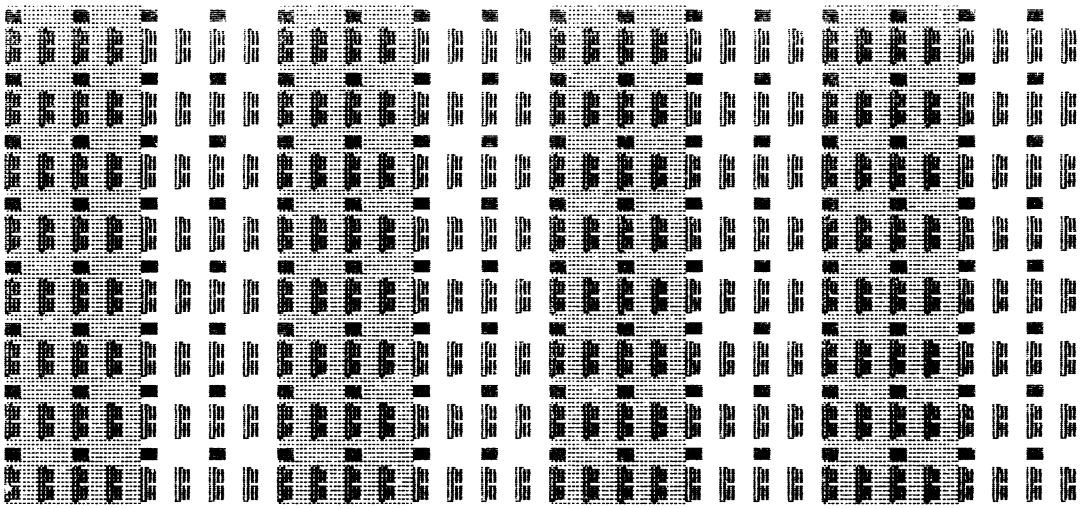

Figure 4-3.

This is an alternating pattern of high-low transitions, low-high transitions, glitches, graticule, and cursor. This is the first pattern for signature analysis.

Characters Exercised.

Data Characters.
High-low/low-high transition characters (Two every eight dots).

Enhancement Characters.
Intensity (alternating every 12 dots).
Graticule (on for 32 dots, then blanked for 32 dots).
Cursor (alternating, on for four dots, off for 12 dots)

Blanking (on for four dots, off for four dots during the time the graticule is off).

Glitches (Two every eight dots).

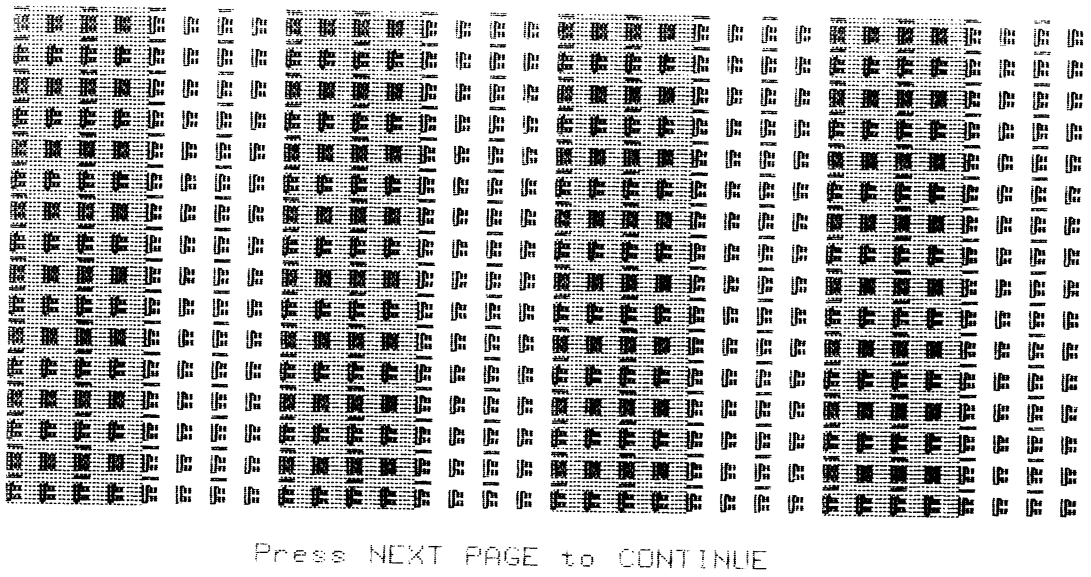

Figure 4-4.

This is the same as the previous pattern, but for 16 channels. This is the second pattern for signature analysis.

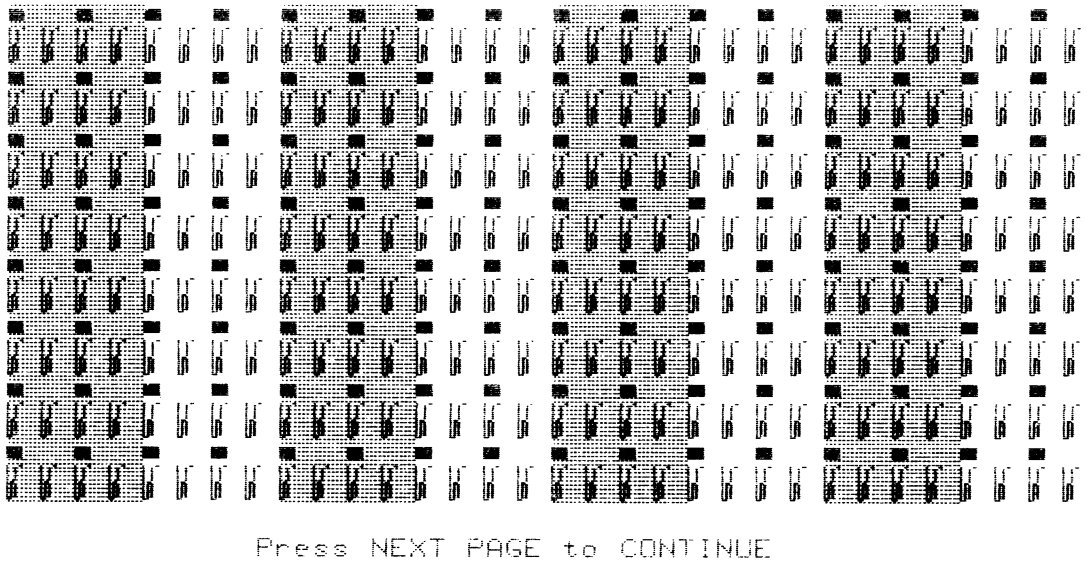

Figure 4-5.

This is the third pattern for signature analysis.

Characters Exercised.

Data Characters.
    High (following every glitch character).
    High-low transition (alternating every eight dots).

Enhancement Characters.
    Cursor (alternating, on for four dots, off for 12 dots).
    Graticule (alternating, continuous for 32 dots, then off for 32 dots).

Dual Threshold (following every high-low transition).

Glitch (following every dual threshold character).

Blanking (lasts for four dots on the part of the display where there is no cursor).

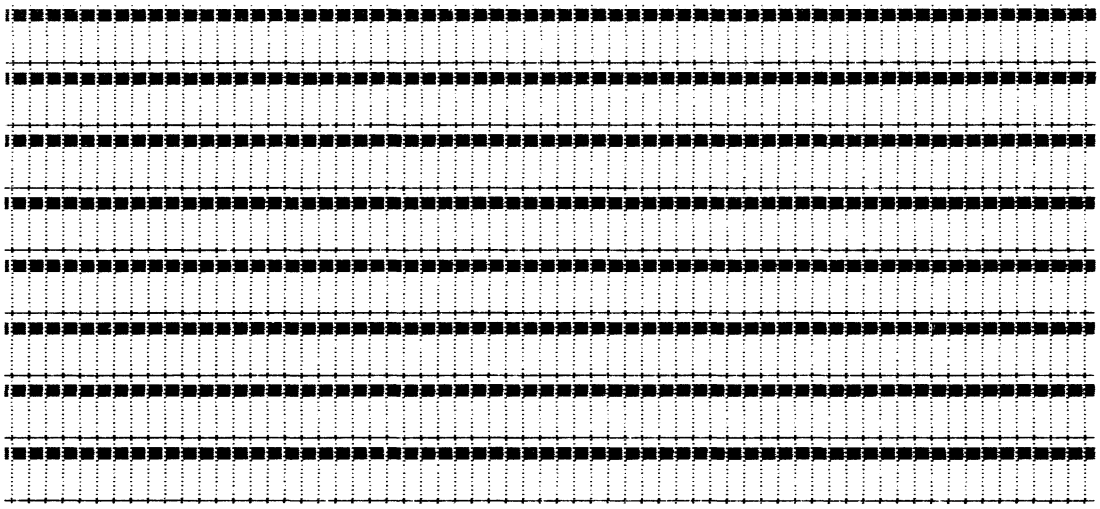

Figure 4-6.

This display is repeated eight times and shifted by one dot.

Characters Exercised.

Data Characters.
    Low (continuous on all channels).

Enhancement Characters.
    Graticule (every fourth dot).
    Cursor (continuous except for graticule columns).

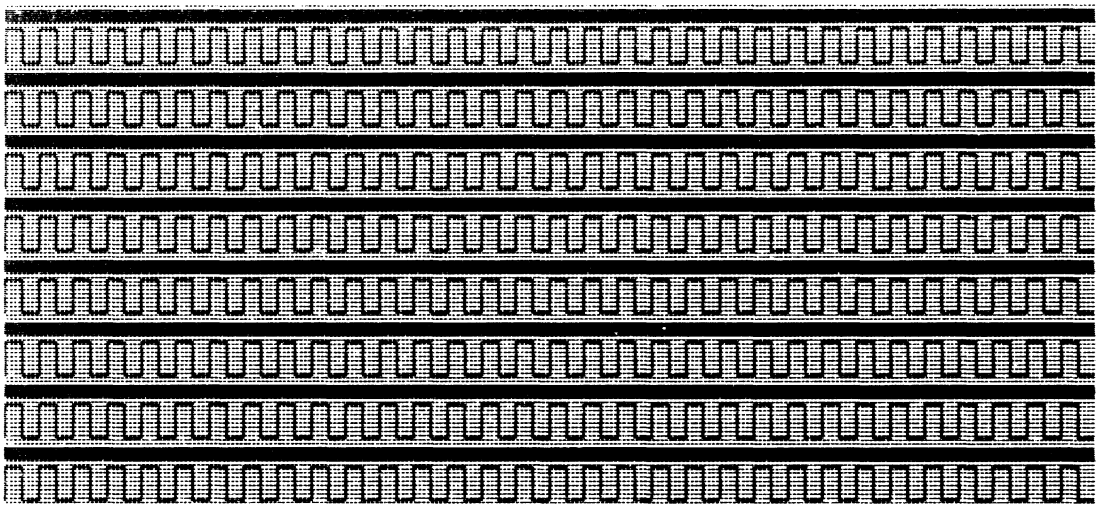

Figure 4-7.

This is a pattern of highs lasting four dots, high-low transitions, lows lasting four dots, and then low-high transitions. This display is shifted by one dot in each of the next eight displays (not shown).

Characters Exercised.

Data Characters.
- High (Alternating every four dots).
- Low (Alternating every four dots).
- High-low transitions.
- Low-high transitions.

Enhancement Characters.
- Graticule (continuous).
- Cursor (continuous).
- Intensify (all).

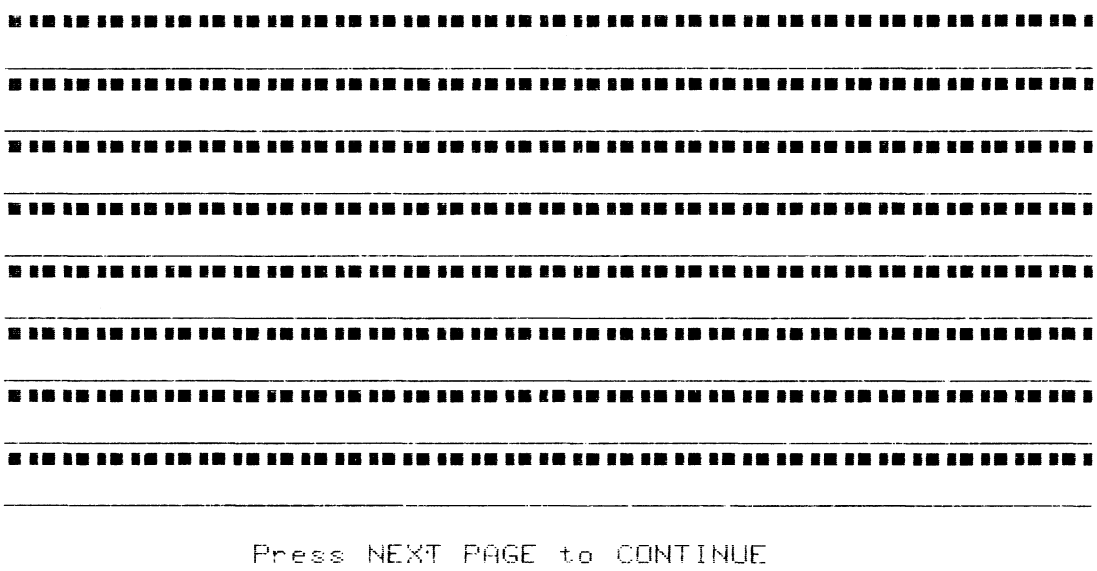

Figure 4-8.

This pattern is displayed eight times and shifted by one dot each time.

Characters Exercised.

Data Characters.
    Low (continuous on all channels).

Enhancement Characters.
    Intensity (alternating pattern imposed on the continuous lows, shifted in each display).
    Cursor (on for four dots, off for two, on for two, off for one, then repeating).

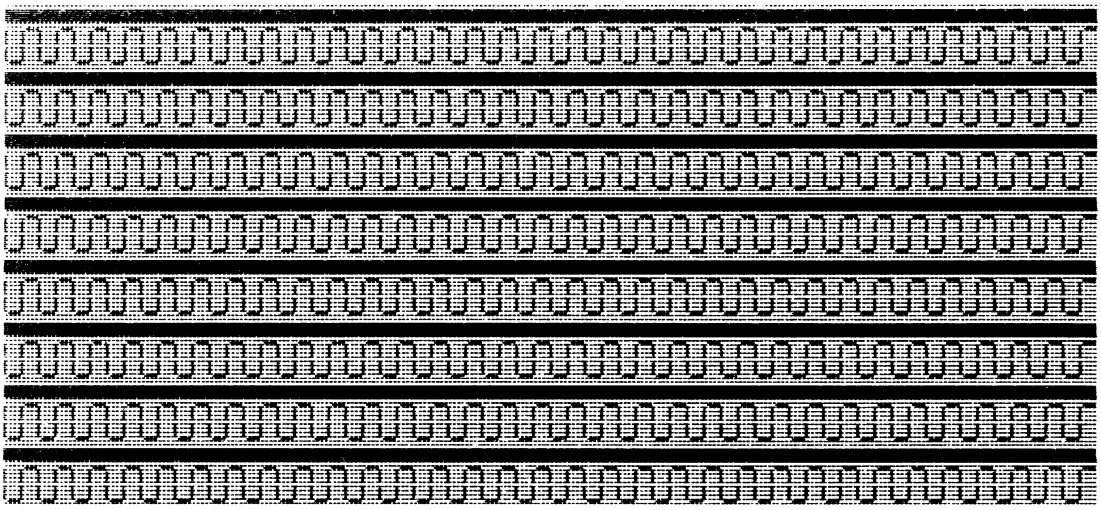

Figure 4-9.

This is a pattern of four highs and a glitch, then four lows and a glitch. The pattern is shifted by one dot in each of the following eight displays.

Characters Exercised.

Data Characters.
    High (lasting four dots, followed by a glitch, then four lows).
    Low (lasting four dots, followed by a glitch, then four highs).

Enhancement Characters.
    Graticule (continuous).
    Cursor (continuous).
    Intensity (all).

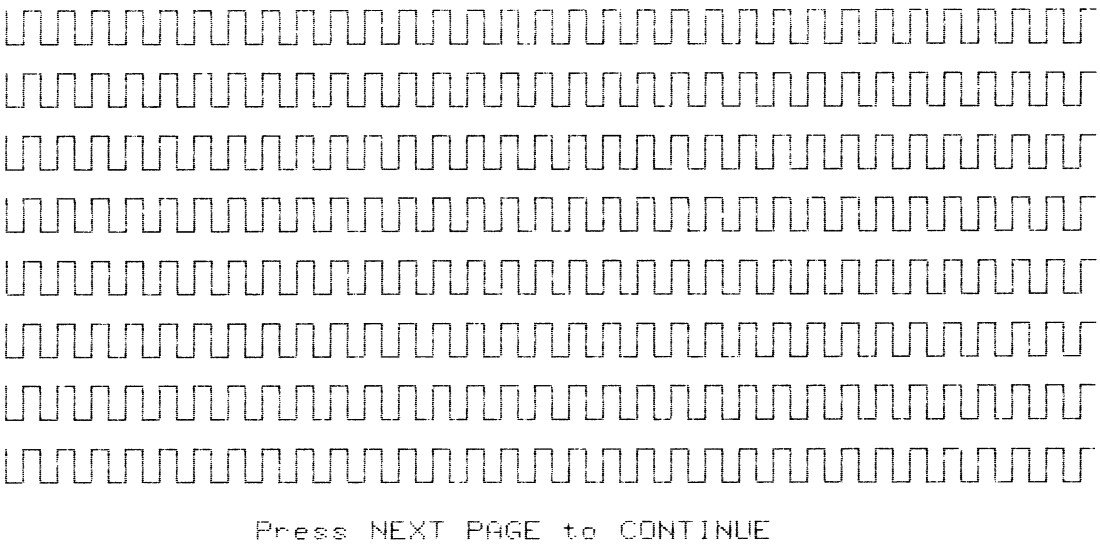

Figure 4-10.

This is a continuous alternation of highs, lows, high-low transitions, and low-high transitions. This pattern is shifted by one dot in each of the following eight displays.

Characters Exercised.

Data Characters.
- High (lasting four dots, followed by a high-low transition).
- Low (lasting four dots, followed by a low-high transition).
- High-low transitions.
- Low-high transitions.

Enhancement Characters.
- None.

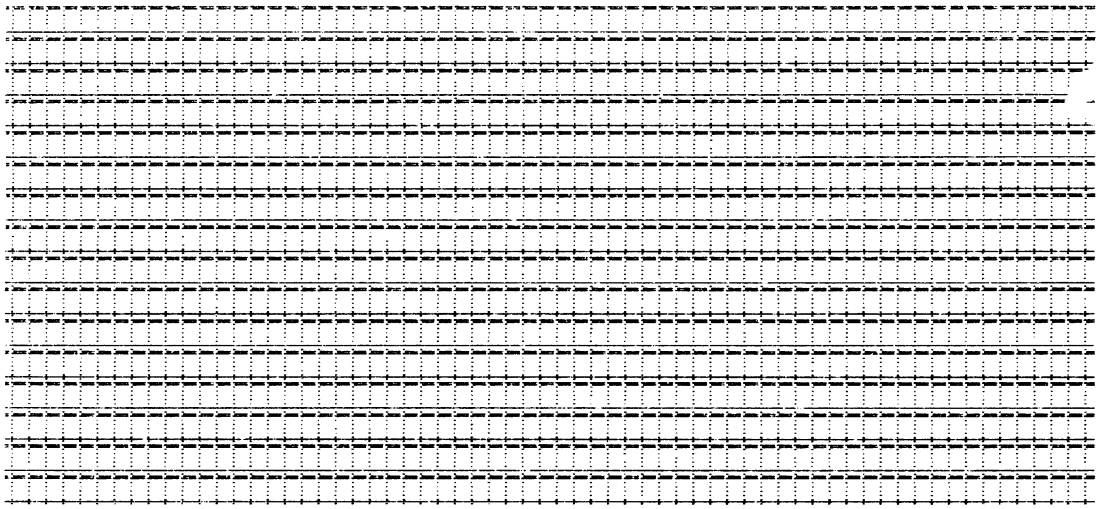

Figure 4-11.

This is the 16-channel version of figure 4-6, shifted by one dot in each of the next eight displays.

Characters Exercised.

Data Characters.
    Low (continuous on every channel).

Enhancement Characters.
    Graticule (every fourth dot).
    Cursor (alternates with the graticule).

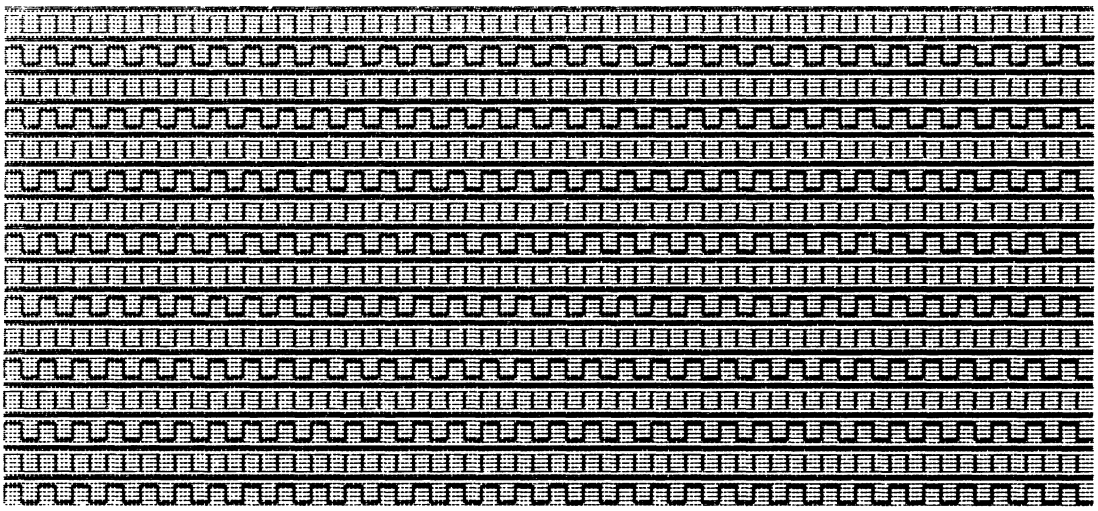

Figure 4-12.

This is the 16-channnel version of figure 4-7, shifted by one dot in each of the next eight patterns. This is a shifting pattern of highs lasting four dots, high-low transitions, lows lasting four dots, and then low-high transitions.

Characters Exercised.

Data Characters.
    High (lasting for four dots, and then alternating with four-dot lows).
    Low (lasting for four dots, and then alternating with four-dot highs).

Enhancement Characters.
    Graticules (continuous).
    Cursor (continuous).
    Intensify (continuous).

Figure 4-13.

This is the 16 channel version of figure 4-8, shifted by one dot in each of the next eight displays.

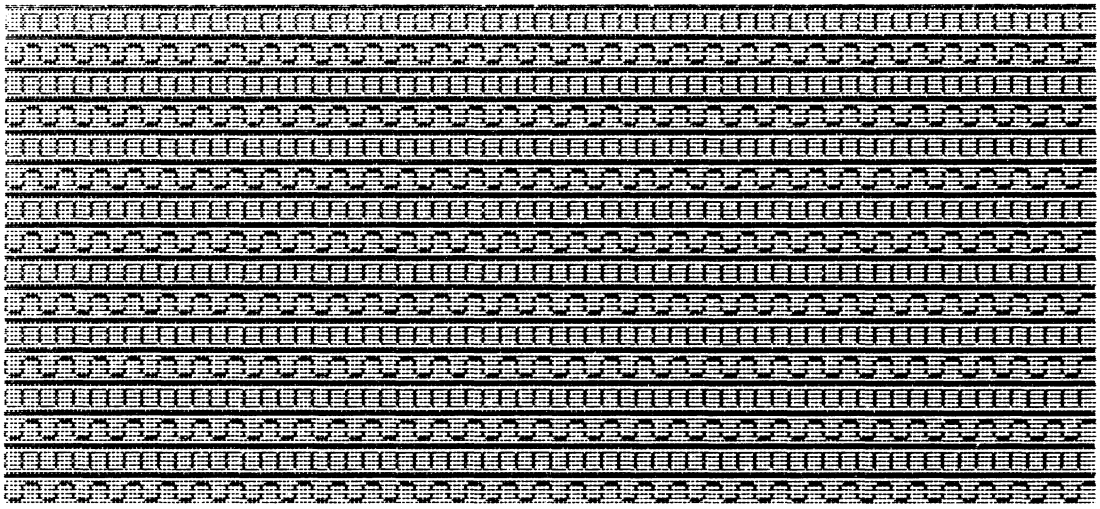

Figure 4-14.

This is the 16-channel version of figure 4-9. The following eight displays are each shifted by one dot. The pattern consists of glitch characters every four dots, followed by highs for four dots, and then lows for four dots. Intensity, cursor, and graticule are continuous.

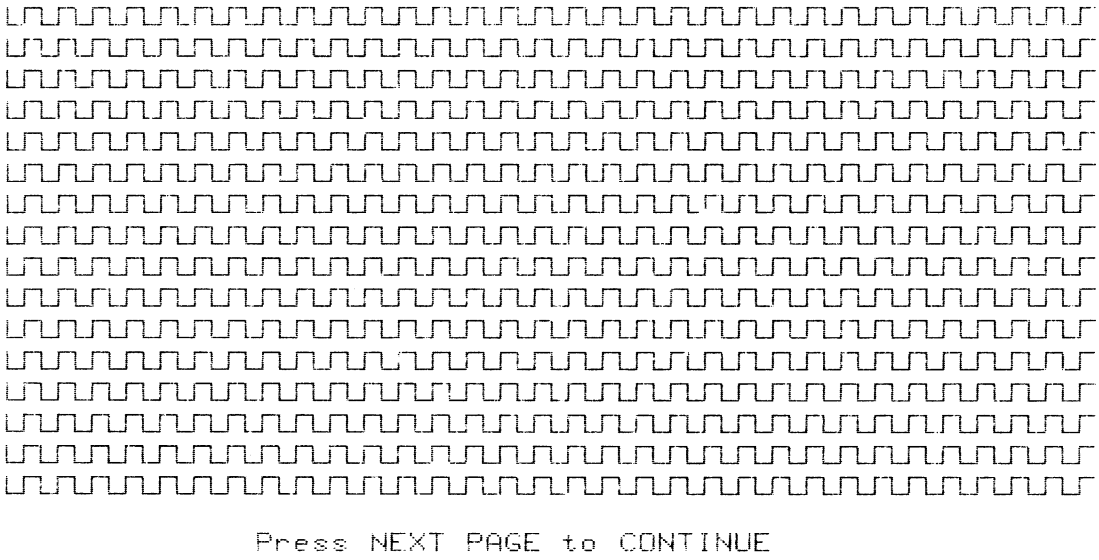

Figure 4-15.

This is the 16 channel version of figure 4-10. It is an alternating pattern of data characters: high, low, high-low transitions, and low-high transitions. The following eight patterns are each shifted by one dot. There are no enhancement characters.

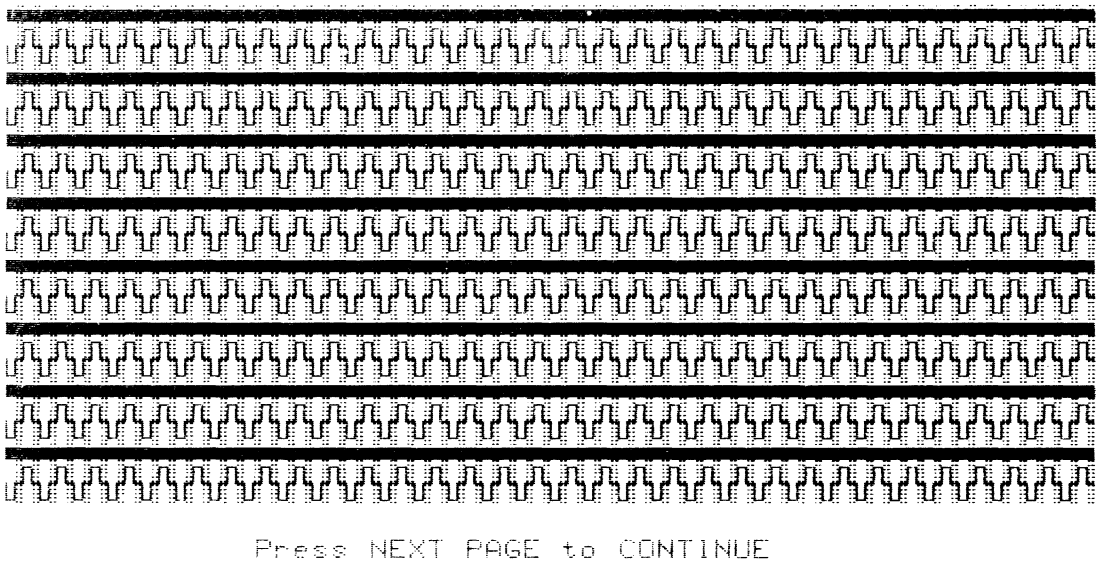

Figure 4-16.

This is an alternating pattern of highs, small transitions, middles, and lows. The pattern is shifted by one dot in the following eight displays.

Characters Exercised.

Data Characters.
- High (alternate with dual threshold and low characters).
- Low (alternate with dual threshold and high characters).

Enhancement Characters.
- Graticule (repeated twice, blanked twice, repeated twice, etc.).
- Cursor (continuous).
- Intensity (cursor is intensified every other two dots, and middles are intensified).

Dual Threshold (alternate with highs and lows).

4-75. INTER MODULE BUS PERFORMANCE VERIFICATION. (Supplementary PV test)

4-76. This is a supplementary PV test. To access this test press the following keys:

a. Press "opt_test"; RETURN

b. Type the timing control board slot number; RETURN

c. Press "test_IMB"; RETURN

d. The screen should show a display like Figure 4-3.

```
Inter Module Bus Performance Verification          Tue, 19 Oct 1982, 11:12

  Slot #  ID #  Module description
  ------  -----  ------------------

     3    1001   200 MHz Timing Analyzer          64601A  TIME_CTL

Board for IMB stimulus
     7    1001   200 MHz Timing Analyzer          64601A  TIME_CTL

IMB test results  (1 = Error)
 RECEIVE 000000 (DCLK,LME,LTE,HTR,RST,HLD)  DRIVE  0000 (BNC4,LME,LTE,HTR)

IMB stimulus board limitations  (1 = Not tested)
  DRIVE  100000 (DCLK,LME,LTE,HTR,LTE,HTR) RECEIVE 1000 (BNC4,LME,LTE,HTR)


  TESTED       0     FAILED       0
```

Figure 4-17. Inter Module Bus Performance Verification.

4-77. For this test, there must be another analyzer, either state or timing, present in the mainframe. One analyzer is the "test" board and the other is the "stimulus" board.

4-78. The test checks each of the IMB lines that are used commonly by the stimulus and test boards. In figure 4-3, slot 3 contains the test board and slot 7 contains the stimulus board.

4-79. All the test board lines that can be driven or received are listed in the display under the heading "IMB test results. When six 0's, 000000, are indicated for RECEIVE, and four 0's are indicated for DRIVE, all IMB lines pass satisfactorily.

4-80. When the particular stimulus board used in the test is unable to drive or receive certain lines, those lines are indicated under the heading "IMB stimulus board limitations". A "1" indicates those lines which cannot be tested. In figure 4-3, for example, the stimulus board in slot 7 cannot drive the DELAY CLOCK line, and cannot receive from the BNC4 external connector. Without this limitation listing, those lines would normally show errors.

4-81. Description.

4-82. DCLK. (Same as HE/DCLK, GMC, PDC).

1. The stimulus board sends ten clocks over this line.
2. The test board must receive ten and only ten clocks.

4-83. LME, LTE, HTR. (Same as LE/ME, LE/TE, LE/TR)

1. These three lines are initialized low.
2. The stimulus board drives one line at a time high.
3. The test board must see a high only on the exercised line.
4. The three lines are initialized high.
5. The stimulus board drives one line at a time low.
6. The test board must see a low only on the exercised line.

4-84. RST, HLD (Same lines as LE/TE, HE/TR)

In the Post Qualify Mode, HTR and LTE have different functions than in the other timing analyzer modes. HTR is a HOLD command from another analyzer over the IMB, and LTE is the RESET command.

In the Post Qualify Mode, the timing analyzer triggers independently; then at some later time, another analyzer can initiate a re-run of the timing analayzer, or tell it to hold its present data.

The Post Qualify Mode, then, consists of three possible states: (1) The NORMAL data acquisition state, in which the timing analyzer is acquiring data while looking for a trigger condition. (2) The HOLD state, in which the timing analyzer has triggered and is told by a second analyzer to hold its data. (3) The RESET state, in which the timing analyzer is told by another analyzer to RESET and watch for another trigger condition.

4-85. POST-QUALIFY MODE -- RESET

1. DACs are set for an "always trigger" condition.
2. Stimulus board drives LTE true.
3. DACs are programmed for a "no trigger" condition.
4. LTE is set false. This should initiate a RESET. Since the DACs are set for "no trigger", the measurement should still be running (incomplete) because LTE did reset the analyzer and there was still no trigger.
5. DACs are set for an "always trigger" condition.
6. The analyzer should trigger and stop the measurement.

4-86. POST-QUALIFY MODE -- HOLD

1. DACs are set for "always trigger".
2. Test board drives HTR true.
3. Stimulus board drives LTE true.
4. DACs are set for "never trigger".
5. Stimulus board drives LTE false. There should still be a trigger because HTR (which is a HOLD line in the POSTQUALIFY mode) is still true. The HOLD prevents a RESTART.
6. The stimulus board now drives HTR true. The timing analyzer is still programmed for the POST-QUALIFY MODE, but it no longer drives HTR.
7. DACs are set for "never trigger".
8. Initiate a HOLD from the stimulus board by driving HTR true.
9. Set the DACs for "always trigger".
10. Verify that HOLD (HTR) prevents a trigger.

4-87. SUPPLEMENTARY BOARD ID TEST.

4-88. The board ID circuits have stable signatures when "opt_test" is pressed. If the Timing Boards are not then listed on the screen, the ID circuitry is not working. Check the ID circuitry signatures at U88 and U89.

4-89. The following figures (4-18 to 4-26) show the operator softkey sequence needed to run a single PV test repeatedly for signature analysis purposes. Each PV test corresponds to one signature loop. Signature lists are given following the figures.

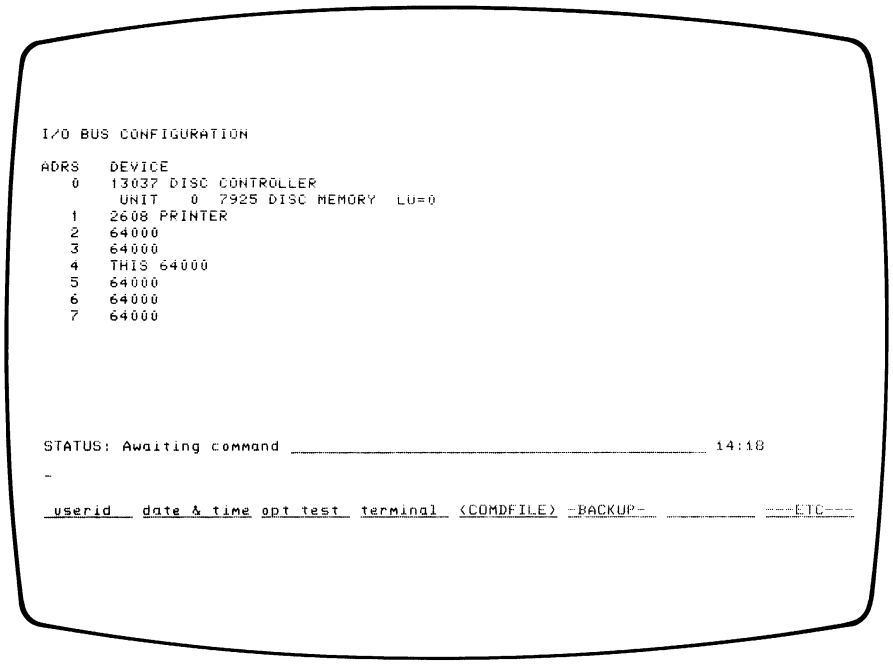

Figure 4-18. Press "opt_test".

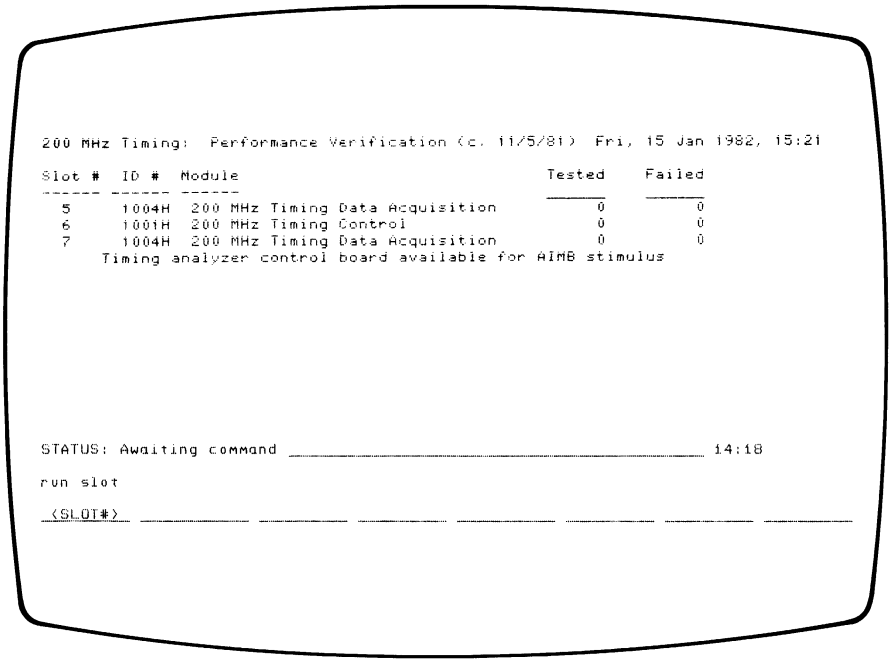

Figure 4-19. Type the slot number.

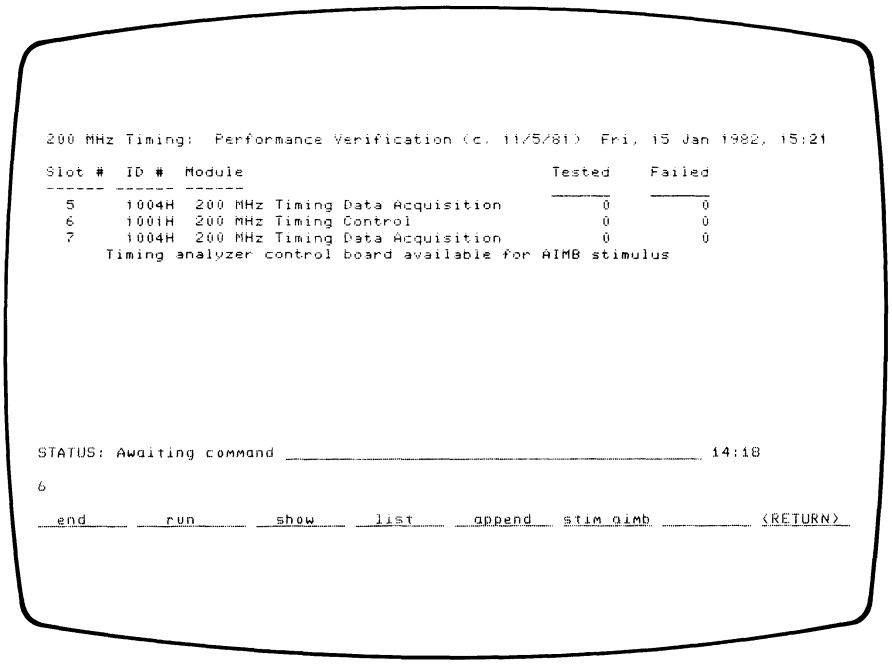

Figure 4-20. Press "run".

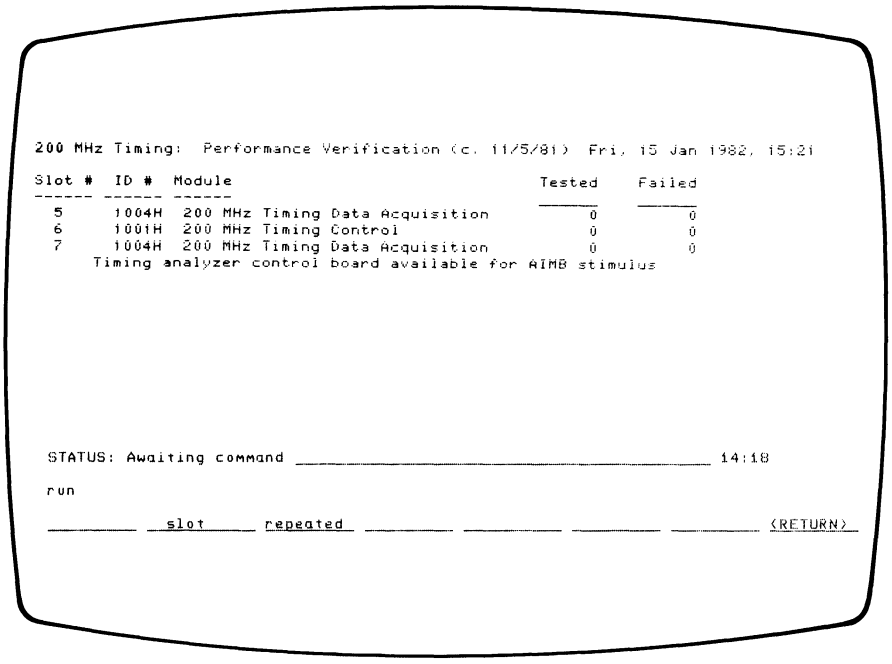

Figure 4-21. Press "slot".

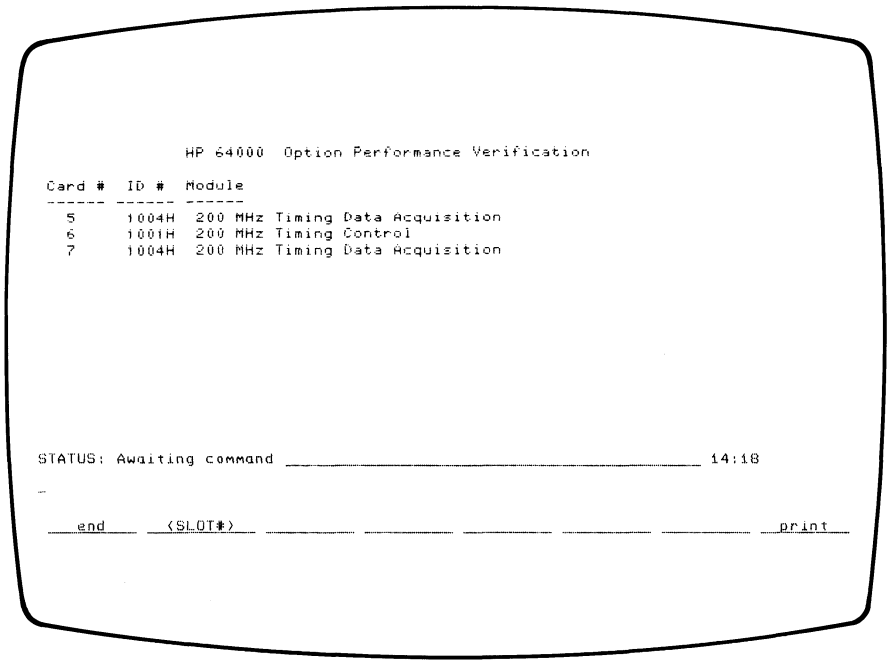

Figure 4-22. Type the slot number.

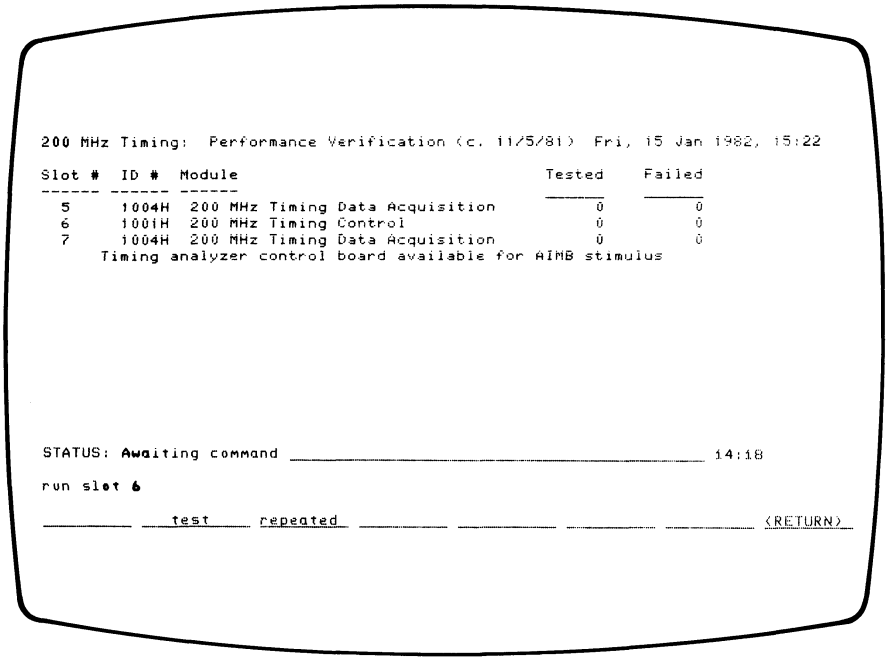

Figure 4-23. Press "test".

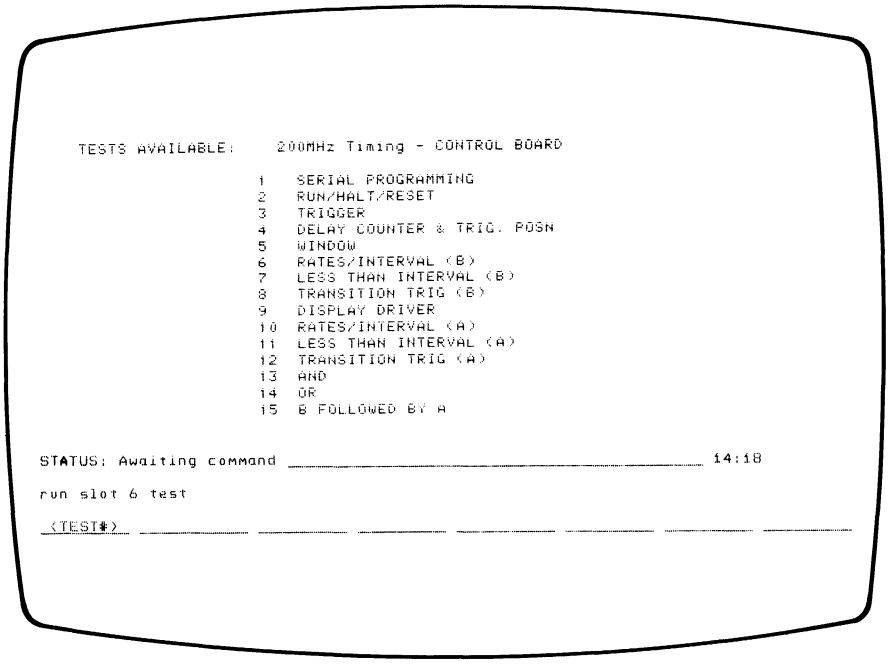

Figure 4-24. Type the test number.

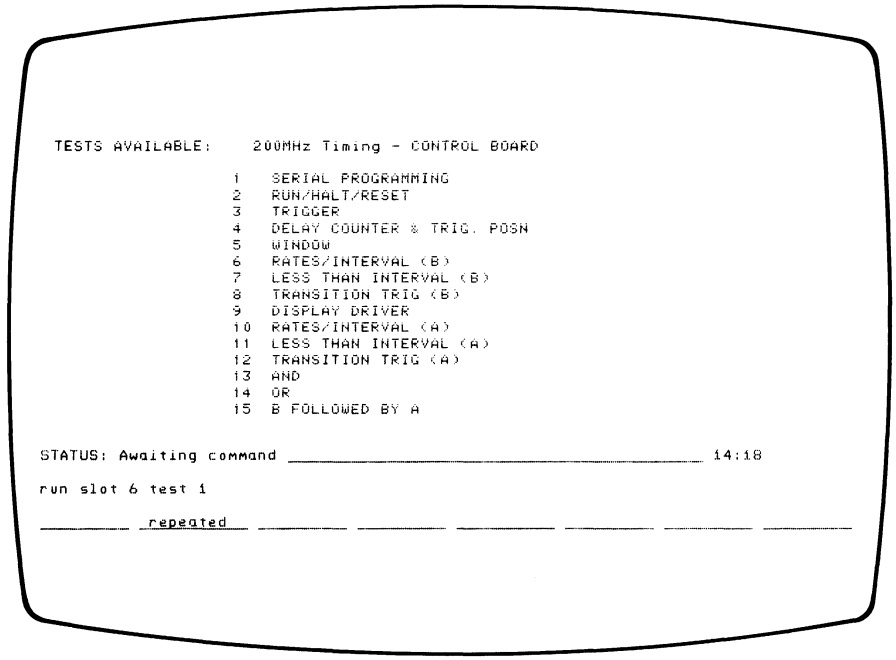

Figure 4-25. Press "repeated".

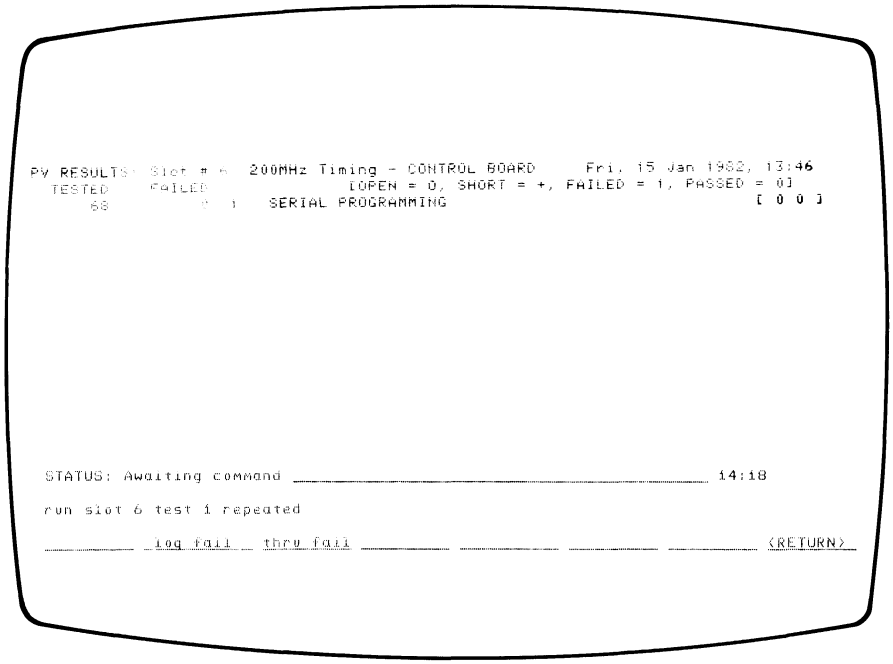

Figure 4-26. Press [RETURN].

4-90. SIGNATURE ANALYSIS

4-91. The following 15 signature loops correspond to the previously given performance verification tests. That is, if a PV test fails, run the signature loop corresponding to that test. For example, if one of the test steps for TEST 1: SERIAL PROGRAMMING shows a "1" instead of a "0" in the bracket, look at the signatures for LOOP 1. In order to take the signatures, run TEST 1 repeatedly, using the procedure illustrated by the above figures (4-18 to 4-26).

64601A Timing Control Board
SERIAL PROGRAMMING #1

NORM MODE VH = 8H96

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 neg. edge
Location of GROUND: gnd

TTL

U 49- 4	A418
U 49- 5	low
U 49-12	low
U 49-13	H75A
U 85- 1	62CA
U 85- 2	A418
U 85- 3	UP50
U 85- 4	low
U 85- 5	117F
U 85- 6	low
U 85- 7	UP50
U 85- 8	low
U 85- 9	UP50
U 85-11	low
U 85-12	UP50
U 85-13	low
U 85-14	UP50
U 85-15	high
U 85-16	UP50
U 85-17	low
U 85-18	3C12
U 85-19	62CA
U 86- 5	73F6
U 86- 6	high
U 86- 7	2471
U 86-10	low
U 86-11	high
U 88- 1	low
U 88- 2	high
U 88- 3	0000
(TOTLZ=0781)	
U 88- 4	8H96
(TOTLZ=0781)	
U 88- 5	0000
(TOTLZ=12257)	
U 88- 6	0000
(TOTLZ=0781)	
U 89- 1	8H96
(TOTLZ=0781)	
U 89- 2	low
U 89- 3	UP50
U 89- 4	8H96
(TOTLZ=0781)	
U 89- 5	low
U 89- 6	3C12
U 91- 1	2471
U 91- 2	2471
U 91- 3	FC5H
U 91- 4	0000
(TOTLZ=12257)	
U 91- 5	0000
(TOTLZ=0781)	
U 91- 6	high
U 91- 7	46FC
U 91- 9	high
U 91-10	high
U 91-11	high
U 91-12	62CA
U 91-13	high
U 91-14	high
U 91-15	2471
U101- 8	73F6
U101- 9	UP50

ECL

U 1- 1	0000
(TOTLZ=0520)	
U 1- 3	0051
U 1- 4	P2CA
U 1- 6	high
U 1- 7	low
U 1- 8	low
U 1- 9	low
U 1-10	low
U 1-12	A9P7
U 1-13	high
U 1-14	A9P7
U 1-15	high
U 1-17	0000
(TOTLZ=0520)	
U 1-18	low
U 1-19	high
U 1-20	high
U 1-24	high
U 4- 7	1776
U 4- 9	6U9C
U 4-14	A9P7
U 5- 4	A418
U 10- 1	high
U 10- 2	6U9C
U 10- 3	1776
U 10- 4	5A1U
U 10- 5	16CC
U 10- 6	6U9C
U 10- 7	1776
U 10- 9	A9P7
U 10-10	5A1U
U 10-11	40PF
U 10-12	P284
U 10-13	40PF
U 10-14	P284
U 10-15	9874
U 11- 1	high

```
U 11- 2  AF14
U 11- 3  C6FF
U 11- 4  HAHH
U 11- 5  9249
U 11- 6  AF14
U 11- 7  C6FF
U 11- 9  A9P7
U 11-10  HAHH
U 11-11  148A
U 11-12  6HC6
U 11-13  148A
U 11-14  6HC6
U 11-15  96AH
U 13- 4  HAHH
U 13- 7  148A
U 13-11  6HC6
U 13-13  96AH
U 15- 1  high
U 15- 2  3AF1
U 15- 3  C88U
U 15- 4  8FC6
U 15- 5  96AH
U 15- 6  3AF1
U 15- 7  C88U
U 15- 9  A9P7
U 15-10  8FC6
U 15-11  PCPH
U 15-12  F711
U 15-13  PCPH
U 15-14  F711
U 15-15  16CC
U 17- 3  P09C
U 17- 4  8FC6
U 17- 7  PCPH
U 17-11  F711
U 17-13  16CC
U 19- 7  H985
U 21- 6  H9C9
U 21-10  802P
U 21-12  1363
U 24- 5  P2CA
U 24- 7  P2CA
U 24-11  40PF
U 24-12  5A1U
U 27- 4  AF14
U 27- 6  8H49
U 27- 7  C6FF
U 34-13  P284
U 35- 7  P284
U 35-13  P284
U 36- 1  0000
(TOTLZ=0520)
U 36- 3  P2CA
U 36- 4  A418
U 36- 6  high
U 36- 7  low
U 36- 8  low
U 36- 9  low
U 36-10  A418
U 36-12  A9P7
U 36-13  high
U 36-14  A9P7
U 36-15  high
U 36-17  0000
(TOTLZ=0520)
U 36-18  low
U 36-19  high
U 36-20  high
U 36-24  high
U 37- 1  0000
(TOTLZ=0520)
U 37- 3  6AHC
U 37- 4  0051
U 37- 6  high
U 37- 7  low
U 37- 8  15P2
U 37- 9  H75A
U 37-10  low
U 37-12  A9P7
U 37-13  high
U 37-14  A9P7
U 37-15  high
U 37-17  0000
(TOTLZ=0520)
U 37-18  low
U 37-19  high
U 37-20  high
U 37-24  high
U 38- 1  0000
(TOTLZ=0520)
U 38- 3  9874
U 38- 4  6AHC
U 38- 6  high
U 38- 7  low
U 38- 8  low
U 38- 9  high
U 38-10  80C2
U 38-12  A9P7
U 38-13  high
U 38-14  A9P7
U 38-15  high
U 38-17  0000
(TOTLZ=0520)
U 38-18  low
U 38-19  high
U 38-20  high
U 38-24  high
U 42- 6  AF14
U 42-12  3AF1
U 43- 4  3AF1
U 43- 7  C88U
U 49- 3  A418
U 49- 7  low
U 49-11  low
U 49-15  H75A
U 50- 9  6AHC
U 54- 5  C33H
U 54- 6  C7PF
U 54-11  79P0
U 55- 4  9249
U 55-11  0051
U 55-13  F145
U 67- 6  6C36
U 67-11  2HUU
U 69- 3  A9P7
U 69- 6  A9P7
U 69- 7  high
U 71- 1  high
U 71- 2  2HUU
U 71- 3  6C36
U 71- 4  1363
U 71- 5  79P0
U 71- 6  2HUU
U 71- 7  6C36
U 71- 9  A9P7
U 71-10  1363
U 71-11  H985
U 71-12  F145
U 71-13  H985
U 71-14  F145
U 71-15  9249
U 73- 1  high
U 73- 2  0178
U 73- 3  802P
U 73- 4  H9C9
U 73- 5  73F6
U 73- 6  0178
U 73- 7  802P
U 73- 9  A9P7
U 73-10  H9C9
U 73-11  C33H
U 73-12  C7PF
U 73-13  C33H
U 73-14  C7PF
U 73-15  79P0
U 74-10  0178
U 74-11  A069
U 74-13  high
U 74-14  high
U 86- 2  73F6
U 86- 3  A9P7
```

64601A Timing Control Board
RUN / HALT / RESET #2

NORM MODE VH = 01UF

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 pos. edge
Location of GROUND: gnd

TTL

U 85- 1	01UF
(TOTLZ=0002)	
U 85- 2	low
U 85- 3	01UF
U 85- 4	low
U 85- 5	01UF
U 85- 6	low
U 85- 7	01UF
U 85- 8	low
U 85- 9	01UF
U 85-12	01UF
U 85-14	01UF
U 85-15	019F
U 85-16	01UF
U 85-17	low
U 85-18	01UF
U 85-19	01UF
(TOTLZ=0002)	
U 86- 5	0000
U 86- 7	high
U 86-10	01UP
U 86-11	019F
U 90- 1	015H
U 90- 2	01U2
U 90- 3	0153
U 90- 4	low
U 90- 5	01UP
U 90- 6	019F
U 90- 7	low
U 90- 9	low
U 90-10	low
U 90-11	low
U 90-12	high
U 90-13	003C
U 90-14	01UF
(TOTLZ=0004)	
U 90-15	high
U 91- 1	01UF
(TOTLZ=0137)	
U 91- 2	01UF
(TOTLZ=0119)	
U 91- 3	01AH
U 91- 4	01UF
(TOTLZ=0255)	
U 91- 5	0000
(TOTLZ=0011)	
U 91- 6	high
U 91- 7	01UF
(TOTLZ=0004)	
U 91- 9	high
U 91-10	hi1h
U 91-11	high
U 91-12	01UF
(TOTLZ=0002)	
U 91-13	high
U 91-14	high
U 91-15	high
U101- 8	0000
U101- 9	01UF

ECL

U 1- 1	low
U 1- 3	high
U 1- 4	low
U 1- 6	high
U 1- 7	low
U 1-12	low
U 1-13	0002
U 1-14	low
U 1-15	high
U 1-17	low
U 1-18	low
U 1-19	high
U 1-20	high
U 1-24	0002
U 5- 5	0002
U 5-13	0002
U 19- 9	0002
U 19-13	0002
U 21-13	0002
U 22- 9	0002
U 23- 4	0002
U 23-12	0002
U 36- 1	low
U 36- 3	low
U 36- 4	low
U 36- 6	high
U 36- 7	low
U 36- 8	0000
U 36- 9	low
U 36-10	low
U 36-12	low
U 36-13	0002
U 36-14	low
U 36-15	high
U 36-17	low
U 36-18	low
U 36-19	high
U 36-20	high

```
U 36-24  0002
U 37- 1  low
U 37- 3  high
U 37- 4  high
U 37- 6  high
U 37- 7  low
U 37- 9  low
U 37-10  low
U 37-12  low
U 37-13  0002
U 37-14  low
U 37-15  high
U 37-17  low
U 37-18  low
U 37-19  high
U 37-20  high
U 37-24  0002
U 38- 1  low
U 38- 3  low
U 38- 4  high
U 38- 6  high
U 38- 7  low
U 38- 8  0000
(TOTLZ=0432)
U 38- 9  high
U 38-10  high
U 38-12  low
U 38-13  0002
U 38-14  low
U 38-17  low
U 38-18  low
U 38-19  high
U 38-20  high
U 38-24  0002
U 51- 4  0002
U 51-12  0002
U 52-12  0002
U 66- 4  0002
U 66-11  0002
U 67- 5  0002
U 67- 9  0002
U 67-12  0002
U 69- 7  0002
U 69- 9  0060
U 69-10  0002
U 69-11  0002
U 69-12  019F
U 69-13  high
U 69-14  019F
U 74-13  0002
U 86- 2  0000
U 86- 3  low
U 86-12  0002
U 86-14  019F
```

64601A Timing Control Board
TRIGGER #3

NORM MODE

VH = 8267

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Temporarily connect U13 pins 12 and 14 together

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 neg. edge
Location of GROUND: gnd

TTL

U 49- 4	8195
U 49- 5	5P64
U 49-12	CFA9
U 49-13	1U26
U 85- 1	HU0C
U 85- 2	8195
U 85- 3	7416
U 85- 4	5P64
U 85- 5	F282
U 85- 6	low
U 85- 7	5663
U 85- 8	low
U 85- 9	723H
U 85-11	2CP3
U 85-12	U3HC
U 85-13	low
U 85-14	U3P5
U 85-15	6P07
U 85-16	3372
U 85-17	CFA9
U 85-18	59UA
U 85-19	HU0C
U 86- 5	0093
U 86- 7	4730
U 86-10	5P64
U 86-11	6P07
U 90- 1	P673
U 90- 2	P67A
U 90- 3	5471
U 90- 4	low
U 90- 5	5P64
U 90- 6	6P07
U 90-12	high
U 90-13	CH35
U 90-14	1725
U 90-15	high
U 91- 1	F82P
U 91- 2	4730
U 91- 3	9542
U 91- 4	0000
U 91- 5	0000
U 91- 6	high
U 91- 7	1725
U 91-12	HU0C
U 91-13	0H79
U 91-15	4730

ECL

U 1- 1	0000
(TOTLZ=0260)	
U 1- 3	3314
U 1- 4	820A
U 1- 6	high
U 1- 7	low
U 1-12	F557
U 1-13	HF03
U 1-14	F557
U 1-15	high
U 1-17	0000
(TOTLZ=0260)	
U 1-18	low
U 1-19	high
U 1-20	high
U 1-24	HF03
U 10- 1	high
U 10- 2	3213
U 10- 3	9909
U 10- 4	0CC4
U 10- 5	57U1
U 10- 6	3213
U 10- 7	9909
U 10- 9	F557
U 10-10	0CC4
U 10-11	81CP
U 10-12	87PU
U 10-13	81CP
U 10-14	87PU
U 10-15	4793
U 11- 1	high
U 11- 2	93AA
U 11- 3	F9H5
U 11- 4	CP55
U 11- 5	1F4C
U 11- 6	93AA
U 11- 7	F9H5
U 11- 9	F557

U 11-10 CP55
U 11-11 F6F1
U 11-12 P360
U 11-13 F6F1
U 11-14 P360
U 11-15 2C0U
U 13- 1 high
U 13- 2 06P4
U 13- 3 8483
U 13- 4 CP55
U 13- 5 low
U 13- 6 low
U 13- 7 F6F1
U 13- 9 low
U 13-10 P2FH
U 13-11 P360
U 13-12 0A14
U 13-13 2C0U
U 13-14 0A14
U 13-15 low
U 15- 1 high
U 15- 2 0F6F
U 15- 3 0636
U 15- 4 59A4
U 15- 5 2C0U
U 15- 6 0F6F
U 15- 7 0636
U 15- 9 F557
U 15-10 59A4
U 15-11 3539
U 15-12 1A9F
U 15-13 3539
U 15-14 1A9F
U 15-15 57U1
U 17- 1 high
U 17- 2 H55H
U 17- 3 573A
U 17- 4 59A4
U 17- 5 low
U 17- 6 low
U 17- 7 3539
U 17- 9 low
U 17-10 P2FH
U 17-11 1A9F
U 17-12 0A14
U 17-13 57U1
U 17-14 0A14
U 17-15 low
U 19- 1 high
U 19- 2 3PFP
U 19- 3 05AC
U 19- 5 CFA9
U 19- 7 4A32
U 19- 9 HF03
U 19-10 CFA9
U 19-11 high
U 19-12 low
U 19-13 HF03
U 19-14 low
U 21- 1 high
U 21- 2 87FF
U 21- 3 5P64
U 21- 5 05AC
U 21- 6 032U
U 21- 7 3PFP
U 21-10 80U6
U 21-11 141U
U 21-12 AU7A
U 21-13 HF03
U 21-14 F6CA
U 21-15 P2FH
U 27- 1 high
U 27- 2 8267
U 27- 3 CFFC
U 27- 4 93AA
U 27- 6 810C
U 27- 7 F9H5
U 27- 9 8267
U 27-11 036F
U 27-12 036F
U 27-13 810C
U 27-14 810C
U 31- 1 -4.52 DCV
U 31- 2 -5.17 DCV
U 31- 3 -5.09 DCV
U 31- 4 -5.17 DCV
U 31- 5 -4.37 DCV
U 31- 6 -4.99 DCV
U 31- 7 -5.17 DCV
U 31- 8 -5.17 DCV
U 31- 9 -1.78 DCV
U 31-10 0.17 DCV
U 31-11 0.01 DCV
U 31-12 -5.17 DCV
U 31-13 0.65 DCV
U 31-14 0.01 DCV
U 31-15 -4.1 DCV
U 31-16 -4.52 DCV
U 32- 1 4.99 DCV
U 32- 2 0.17 DCV
U 32- 3 0.01 DCV
U 32- 4 0.17 DCV
U 32- 5 4.99 DCV
U 32- 6 0.17 DCV
U 32- 7 0.01 DCV
U 32- 8 4.99 DCV
U 32- 9 0.17 DCV
U 32-10 0.01 DCV
U 32-11 4.99 DCV
U 32-12 0.17 DCV
U 32-13 0.01 DCV
U 32-14 4.99 DCV
U 34- 1 high
U 34- 2 810C
U 34- 3 036F
U 34- 4 810C
U 34- 6 52C2
U 34- 7 H0H5
U 34- 9 52C2
U 34-11 0000
U 34-12 0000
U 34-13 87PU
U 34-14 0588
U 35- 1 high
U 35- 2 036F
U 35- 3 810C
U 35- 4 0588
U 35- 5 06P4
U 35- 6 8483
U 35- 7 87PU
U 35- 9 low
U 35-10 0588
U 35-11 H55H
U 35-12 573A
U 35-13 87PU
U 35-14 52C2
U 35-15 H0H5
U 36- 1 0000
(TOTLZ=0260)
U 36- 3 820A
U 36- 4 8195
U 36- 6 high
U 36- 7 low
U 36- 8 2CP3
U 36- 9 2CP3
U 36-10 8195
U 36-12 F557
U 36-13 HF03
U 36-14 F557
U 36-15 high
U 36-17 0000
(TOTLZ=0260)
U 36-18 low
U 36-19 high
U 36-20 high
U 36-24 HF03
U 37- 1 0000
(TOTLZ=0260)
U 37- 3 133A
U 37- 4 3314
U 37- 6 high
U 37- 7 low

U 37- 8 PP17
U 37- 9 1U26
U 37-10 7U42
U 37-12 F557
U 37-13 HF03
U 37-14 F557
U 37-15 high
U 37-17 0000
(TOTLZ=0260)
U 37-18 low
U 37-19 high
U 37-20 high
U 37-24 HF03
U 38- 1 0000
(TOTLZ=0260)
U 38- 3 4793
U 38- 4 133A
U 38- 6 high
U 38- 7 low
U 38- 8 2CP3
U 38- 9 high
U 38-10 98A2
U 38-12 F557
U 38-13 HF03
U 38-14 F557
U 38-15 high
U 38-17 0000
(TOTLZ=0260)
U 38-18 low
U 38-19 high
U 38-20 high
U 38-24 HF03
U 39- 1 PP17
U 39- 5 A984
U 39- 6 low
U 39- 9 4793
U 40- 1 high
U 40- 3 0000
(TOTLZ=0003)
U 40- 5 HF03
U 40- 7 0000
U 40- 9 A984
U 40-10 2CP3
U 40-11 0000
U 40-12 HF03
U 40-14 2CP3
U 42- 1 high
U 42- 3 9H49
U 42- 4 high
U 42- 5 CFFC
U 42- 6 93AA
U 42- 7 810C
U 42- 9 low
U 42-10 high
U 42-11 4U5F
U 42-12 0F6F
U 42-13 52C2
U 42-14 CP03
U 42-15 3F64
U 43- 1 high
U 43- 2 high
U 43- 3 4U5F
U 43- 4 0F6F
U 43- 6 52C2
U 43- 7 0636
U 43- 9 high
U 43-11 H0H5
U 43-12 H0H5
U 43-13 52C2
U 43-14 52C2
U 46- 1 -4.53 DCV
U 46- 2 -5.17 DCV
U 46- 3 -5.11 DCV
U 46- 4 -5.17 DCV
U 46- 5 -4.37 DCV
U 46- 6 -4.97 DCV
U 46- 7 -5.17 DCV
U 46- 8 -5.17 DCV
U 46- 9 -1.76 DCV
U 46-10 0.16 DCV
U 46-11 0.01 DCV
U 46-12 -5.17 DCV
U 46-13 0.64 DCV
U 46-14 0.01 DCV
U 46-15 -4.37 DCV
U 46-16 -4.53 DCV
U 47- 1 4.99 DCV
U 47- 2 0.16 DCV
U 47- 3 0.01 DCV
U 47- 4 0.16 DCV
U 47- 5 4.99 DCV
U 47- 6 0.16 DCV
U 47- 7 0.01 DCV
U 47- 8 4.99 DCV
U 47- 9 0.16 DCV
U 47-10 0.01 DCV
U 47-11 4.99 DCV
U 47-12 0.16 DCV
U 47-13 0.01 DCV
U 47-14 4.99 DCV
U 49- 3 8195
U 49- 7 5P64
U 49-11 CFA9
U 49-15 1U26
U 50- 1 high
U 50- 2 5P64
U 50- 4 5P64
U 50- 7 low
U 50- 9 133A
U 50-10 low
U 50-11 3PFP
U 50-12 high
U 50-14 5P64
U 51- 1 high
U 51- 2 2CP3
U 51- 4 HF03
U 51- 6 A984
U 51- 7 5P64
U 51-10 A984
U 51-11 5P64
U 51-12 HF03
U 51-14 low
U 52- 1 high
U 52- 2 low
U 52- 3 2CP3
U 52- 5 high
U 52- 6 2CP3
U 52-12 HF03
U 52-13 A984
U 54- 1 high
U 54- 2 FPC5
U 54- 3 FPC5
U 54- 4 98A2
U 54- 5 187F
U 54- 6 5681
U 54- 7 87FF
U 54- 9 HF03
U 54-10 F6CA
U 54-11 P814
U 54-12 FPC5
U 54-13 low
U 54-14 FPC5
U 54-15 4FH2
U 55- 1 high
U 55- 2 1U26
U 55- 4 1F4C
U 55- 5 9H49
U 55- 6 low
U 55- 7 low
U 55- 9 4FH2
U 55-10 low
U 55-11 3314
U 55-12 P2FH
U 55-13 3896
U 55-14 CP03
U 55-15 low
U 66- 1 high
U 66- 2 5P64
U 66- 3 HF03
U 66- 4 HF03
U 66- 5 7U42
U 66- 6 5P64

U 66- 7	low
U 66- 9	low
U 66-10	98A2
U 66-11	HF03
U 66-12	low
U 66-13	high
U 66-14	6099
U 66-15	5P64
U 67- 1	high
U 67- 2	P2FH
U 67- 3	CFA9
U 67- 4	3F64
U 67- 5	HF03
U 67- 6	563F
U 67- 7	HF03
U 67- 9	HF03
U 67-10	5P64
U 67-11	2AH1
U 67-12	HF03
U 67-14	141U
U 69- 1	high
U 69- 2	low
U 69- 3	F557
U 69- 4	8U8H
U 69- 5	CFA9
U 69- 6	F557
U 69- 7	6P01
U 69- 9	2CP3
U 69-10	HF03
U 69-11	HF03
U 69-12	A984
U 69-13	high
U 69-14	A984
U 71- 1	high
U 71- 2	2AH1
U 71- 3	563F
U 71- 4	AU7A
U 71- 5	P814
U 71- 6	2AH1
U 71- 7	563F
U 71- 9	F557
U 71-10	AU7A
U 71-11	4A32
U 71-12	3896
U 71-13	4A32
U 71-14	3896
U 71-15	1F4C
U 73- 1	high
U 73- 2	8U8H
U 73- 3	80U6
U 73- 4	032U
U 73- 5	0093
U 73- 6	8U8H
U 73- 7	80U6
U 73- 9	F557
U 73-10	032U
U 73-11	187F
U 73-12	5681
U 73-13	187F
U 73-14	5681
U 73-15	P814
U 74- 1	high
U 74- 2	P2FH
U 74- 4	HF03
U 74- 5	P2FH
U 74-10	8U8H
U 74-11	141U
U 74-12	low
U 74-13	HF03
U 74-14	high
U 86- 2	0093
U 86- 3	F557
U 86-12	HF03
U 86-14	A984

64601A Timing Control Board
DELAY COUNTER & TRIG POSITION #4

NORM MODE

VH = 5525

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Temporarily connect U13 pins 12 and 14 together

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 neg. edge
Location of GROUND: gnd

TTL

U 49- 4	3H26
U 49- 5	7331
U 49-12	CU81
U 49-13	38UU
U 64- 4	low
U 64- 5	3PP9
U 64-12	584U
U 64-13	CU81
U 85- 1	5531
U 85- 2	3H26
U 85- 3	75P9
U 85- 4	7331
U 85- 5	6H2U
U 85- 6	UH28
U 85- 7	0052
U 85- 8	CU81
U 85- 9	P53H
U 85-11	584U
U 85-12	7742
U 85-13	3PP9
U 85-14	7396
U 85-15	4019
U 85-16	6HUU
U 85-17	CU81
U 85-18	67F1
U 85-19	5531
U 90- 1	C1CP
U 90- 2	9205
U 90- 3	7195
U 90- 4	low
U 90- 5	H517
U 90- 6	4019
U 90-12	high
U 90-13	6H3H
U 90-14	8P22
U 90-15	high
U 91- 1	HC13
U 91- 2	58F1
U 91- 3	HC07
U 91- 4	0000
(TOTLZ=0199)	
U 91- 5	0000
U 91- 6	high
U 91- 7	8P22
U 91-12	5531
U 91-13	H6U7
U 91-15	58F1
U101- 8	1FH6
U101- 9	49U3

ECL

U 7- 1	high
U 7- 2	23P7
U 7- 3	76F2
U 7- 4	23P7
U 7- 5	76F2
U 7- 9	23P7
U 7-10	76F2
U 7-12	23P7
U 7-13	76F2
U 7-15	76F2
U 36- 1	0000
U 36- 3	25HC
U 36- 6	high
U 36- 7	low
U 36- 8	66A6
U 36- 9	0080
U 36-12	P5A1
U 36-13	8032
U 36-14	P5A1
U 36-15	high
U 36-17	0000
U 36-18	low
U 36-19	high
U 36-20	high
U 36-24	8032
U 37- 1	0000
U 37- 3	1P20
U 37- 4	UH94
U 37- 6	high
U 37- 7	low
U 37- 8	920C
U 37- 9	38UU
U 37-10	0000
U 37-12	P5A1
U 37-13	8032
U 37-14	P5A1
U 37-15	high
U 37-17	0000

U 37-18 low
U 37-19 high
U 37-20 high
U 37-24 8032
U 38- 1 0000
U 38- 3 P4F9
U 38- 4 1P20
U 38- 6 high
U 38- 7 low
U 38- 8 66A6
U 38- 9 high
U 38-10 F708
U 38-12 P5A1
U 38-13 8032
U 38-14 P5A1
U 38-15 high
U 38-17 0000
U 38-18 low
U 38-19 high
U 38-20 high
U 38-24 8032
U 40- 1 high
U 40- 3 P7FP
U 40- 5 8032
U 40- 7 P7FP
U 40- 9 76F2
U 40-10 66A6
U 40-11 P7FP
U 40-12 8032
U 40-14 66A6
U 49- 3 3H26
U 49- 7 7331
U 49-11 CU81
U 49-15 38UU
U 50- 1 high
U 50- 2 7331
U 50- 4 7331
U 50- 7 low
U 50- 9 1P20
U 50-10 low
U 50-11 PAA4
U 50-12 high
U 50-14 7331
U 51- 1 high
U 51- 2 0080
U 51- 4 8032
U 51- 6 76F2
U 51- 7 7331
U 51- 9 low
U 51-10 76F2
U 51-11 7331
U 51-12 8032
U 51-14 CU81
U 51-15 high

U 52- 1 high
U 52- 2 3PP9
U 52- 3 584U
U 52- 5 high
U 52- 6 0080
U 52-12 8032
U 52-13 76F2
U 55- 1 high
U 55- 2 38UU
U 55- 4 78FF
U 55- 5 0P1U
U 55- 6 low
U 55- 7 low
U 55- 9 2U62
U 55-10 low
U 55-11 UH94
U 55-12 6A96
U 55-13 0PU7
U 55-14 70C3
U 64- 3 0000
U 64- 7 3PP9
U 64-11 584U
U 64-15 CU81
U 66- 1 high
U 66- 2 7331
U 66- 3 2614
U 66- 4 8032
U 66- 5 0000
U 66- 6 H517
U 66-10 F708
U 66-11 8032
U 66-15 H517

64601A Timing Control Board
WINDOW COUNTER #5

NORM MODE

VH = 13H2

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Temporarily connect U13 pins 12 and 14 together

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 neg. edge
Location of GROUND: gnd

TTL

U 49- 4	CH73
U 49- 5	A5U7
U 49-12	low
U 49-13	A0P9
U 64- 4	low
U 64- 5	A5A9
U 64-12	8F85
U 64-13	low
U 85- 1	P01U
U 85- 2	CH73
U 85- 3	8226
U 85- 4	A5U7
U 85- 5	P8F9
U 85- 6	429A
U 85- 7	H641
U 85- 8	low
U 85- 9	37H6
U 85-11	8F85
U 85-12	C62A
U 85-13	A5A9
U 85-14	0PFU
U 85-15	5284
U 85-16	0UU2
U 85-17	low
U 85-18	1921
U 85-19	P01U
U 86- 5	49U6
U 86- 7	6A7U
U 86-10	C6HA
U 86-11	5284
U 90- 1	C8A2
U 90- 2	8485
U 90- 3	4U2P
U 90- 4	low
U 90- 5	C6HA
U 90- 6	5284
U 90- 7	low
U 90- 9	low
U 90-10	low
U 90-11	low
U 90-12	high
U 90-13	46HH
U 90-14	5515
U 90-15	high
U 91- 1	C50A
U 91- 2	6A7U
U 91- 3	46F7
U 91- 4	0000
U 91- 5	0000
U 91- 6	high
U 91- 7	5515
U 91- 9	high
U 91-10	high
U 91-11	high
U 91-12	P01U
U 91-13	FFA7
U 91-14	high
U 91-15	6A7U

ECL

U 7- 1	high
U 7- 2	FU99
U 7- 3	HF4C
U 7- 4	FU99
U 7- 5	HF4C
U 7- 9	FU99
U 7-10	HF4C
U 7-11	0000
U 7-12	FU99
U 7-13	HF4C
U 7-15	HF4C
U 19- 1	high
U 19- 2	high
U 19- 3	3FA7
U 19- 4	low
U 19- 5	low
U 19- 7	CC99
U 19- 9	A508
U 19-10	low
U 19-11	high
U 19-12	low
U 19-13	A508
U 19-14	low
U 19-15	13H2
U 21- 1	high
U 21- 2	2U75
U 21- 3	A5U7
U 21- 4	low
U 21- 5	3FA7
U 21- 6	F583
U 21- 7	high
U 21-10	CU70
U 21-11	6CA8
U 21-12	7733
U 21-13	A508
U 21-14	0AU3
U 21-15	C6HA
U 36- 1	0000

U 36- 3 13AP
U 36- 4 CH73
U 36- 6 high
U 36- 7 low
U 36- 8 6PP4
U 36- 9 869U
U 36-10 CH73
U 36-12 6HH9
U 36-13 A508
U 36-14 6HH9
U 36-15 high
U 36-17 0000
U 36-18 low
U 36-19 high
U 36-20 high
U 36-24 A508
U 37- 1 0000
U 37- 3 2H21
U 37- 4 C41P
U 37- 6 high
U 37- 7 low
U 37- 8 0C80
U 37- 9 A0P9
U 37-10 A5U7
U 37-12 6HH9
U 37-13 A508
U 37-14 6HH9
U 37-15 high
U 37-17 0000
U 37-18 low
U 37-19 high
U 37-20 high
U 37-24 A508
U 38- 1 0000
U 38- 3 H7FC
U 38- 4 2H21
U 38- 6 high
U 38- 7 low
U 38- 8 6PP4
U 38- 9 high
U 38-10 94PF
U 38-12 6HH9
U 38-13 A508
U 38-14 6HH9
U 38-15 high
U 38-17 0000
U 38-18 low
U 38-19 high
U 38-20 high
U 38-24 A508
U 39- 1 0C80
U 39- 5 HF4C
U 39- 6 low
U 39- 9 H7FC
U 40- 1 high
U 40- 3 1UU1
U 40- 4 low
U 40- 5 A508
U 40- 6 low
U 40- 7 1UU1
U 40- 9 HF4C
U 40-10 6PP4
U 40-11 1UU1
U 40-12 A508
U 40-13 low
U 40-14 6PP4
U 49- 3 CH73
U 49- 7 A5U7
U 49-11 low
U 49-15 A0P9
U 50- 1 high
U 50- 2 A5U7
U 50- 4 A5U7
U 50- 9 2H21
U 50-11 high
U 50-14 A5U7
U 51- 1 high
U 51- 2 869U
U 51- 4 A508
U 51- 6 HF4C
U 51- 7 A5U7
U 51-10 HF4C
U 51-11 A5U7
U 51-12 A508
U 51-14 low
U 52- 1 high
U 52- 2 A5A9
U 52- 3 8F85
U 52- 5 high
U 52- 6 869U
U 52-12 A508
U 52-13 HF4C
U 55- 1 high
U 55- 2 A0P9
U 55- 4 2PP6
U 55- 5 PHHU
U 55- 6 low
U 55- 7 low
U 55- 9 FC45
U 55-10 low
U 55-11 C41P
U 55-12 A5U7
U 55-13 5HFF
U 55-14 734C
U 55-15 low
U 64- 3 0000
U 64- 7 A5A9
U 64-11 8F85
U 64-15 low
U 66- 1 high
U 66- 2 A5U7
U 66- 3 C625
U 66- 4 A508
U 66- 5 A5U7
U 66- 6 A5U7
U 66-10 94PF
U 66-11 A508
U 66-13 high
U 66-15 A5U7
U 69- 3 6HH9
U 69- 6 79AH
U 69- 7 5284
U 69- 9 APPF
U 69-12 CH3P
U 86- 2 49U6
U 86- 3 79AH
U 86-12 A508
U 86-14 CH3P

64601A Timing Control Board
RATES / INTERVAL B #6

NORM MODE

VH = F036

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Temporarily connect U13 pins 12 and 14 together

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 pos. edge
Location of GROUND: gnd

TTL

U 44- 1	high
U 44- 2	4999
U 44- 3	8CC2
U 44- 4	F74C
U 44- 5	159C
U 44- 6	3P42
U 44- 7	C88C
U 44- 8	C70H
U 44- 9	0HFA
U 44-11	F036
U 44-12	AUCF
U 44-13	F1F1
U 44-14	H3A9
U 44-15	3P30
U 44-16	3078
U 44-17	3299
U 44-18	C233
U 44-19	low
U 49- 4	692C
U 49- 5	U7F0
U 49-12	low
U 49-13	69C9
U 85- 1	F036
U 85- 2	692C
U 85- 3	0P0P
U 85- 4	U7F0
U 85- 5	U5PH
U 85- 6	low
U 85- 7	U1C5
U 85- 9	5P4A
U 85-12	4A31
U 85-14	6FCU
U 85-15	5FA5
U 85-16	CCU5
U 85-17	low
U 85-18	H18U
U 85-19	F036
U 86- 5	7205
U 86- 7	F036
U 86-10	U7F0
U 86-11	5FA5
U 90- 1	2F7F
U 90- 2	6914
U 90- 3	7466
U 90- 4	low
U 90- 5	U7F0
U 90- 6	5FA5
U 90-13	3299
U 90-14	F036
U 90-15	high
U 91- 1	63C9
U 91- 2	884H
U 91- 3	947H
U 91- 4	F036
(TOTLZ=0207)	
U 91- 5	0000
U 91- 6	high
U 91- 7	F036
(TOTLZ=0001)	
U 91-12	F036
U 91-13	F036
U 91-15	F036

ECL

U 7- 1	high
U 7- 2	49P7
U 7- 3	89H1
U 7- 4	49P7
U 7- 5	89H1
U 7- 9	49P7
U 7-10	89H1
U 7-12	49P7
U 7-13	89H1
U 7-15	89H1
U 10- 1	high
U 10- 2	6AH1
U 10- 3	9C4H
U 10- 4	8F06
U 10- 5	0877
U 10- 6	6AH1
U 10- 7	9C4H
U 10-10	8F06
U 10-11	8225
U 10-12	045C
U 10-13	8225
U 10-14	045C
U 10-15	460C
U 15- 1	high
U 15- 2	5FA3
U 15- 3	AP51
U 15- 4	3323
U 15- 5	310A
U 15- 6	5FA3
U 15- 7	AP51
U 15-10	3323
U 15-11	39CF
U 15-12	H8U8
U 15-13	39CF
U 15-14	H8U8
U 15-15	0877
U 17- 1	high
U 17- 2	C6CC

U 17- 3	768H
U 17- 4	3323
U 17- 5	low
U 17- 6	low
U 17- 7	39CF
U 17- 9	low
U 17-10	U7F0
U 17-11	H8U8
U 17-12	0000
U 17-13	0877
U 17-14	0000
U 17-15	low
U 34- 1	high
U 34-13	045C
U 34-14	F46H
U 34-15	F036
U 35-10	F46H
U 35-11	C6CC
U 35-12	768H
U 35-13	045C
U 35-15	72H6
U 36- 1	0000
U 36- 3	9U2U
U 36- 4	692C
U 36- 6	high
U 36- 7	low
U 36- 9	49P7
U 36-10	692C
U 36-12	0000
U 36-13	37U6
U 36-14	0000
U 36-15	high
U 36-17	0000
U 36-18	low
U 36-19	high
U 36-20	high
U 36-24	37U6
U 37- 1	0000
U 37- 3	UC45
U 37- 4	71P0
U 37- 6	high
U 37- 7	low
U 37- 8	FUHA
U 37- 9	69C9
U 37-10	7337
U 37-12	0000
U 37-13	37U6
U 37-14	0000
U 37-15	high
U 37-17	0000
U 37-18	low
U 37-19	high
U 37-20	high
U 37-24	37U6
U 38- 1	0000
U 38- 3	460C
U 38- 4	UC45
U 38- 6	high
U 38- 7	low
U 38- 9	high
U 38-10	9F01
U 38-12	0000
U 38-13	37U6
U 38-14	0000
U 38-15	high
U 38-17	0000
U 38-18	low
U 38-19	high
U 38-20	high
U 38-24	37U6
U 43- 1	high
U 43- 2	high
U 43- 4	5FA3
U 43- 5	low
U 43- 7	AP51
U 43- 9	high
U 43-10	low
U 43-11	72H6
U 43-12	72H6
U 43-13	C2P0
U 43-14	C2P0
U 43-15	0000
U 49- 3	692C
U 49- 7	U7F0
U 49-11	low
U 49-15	69C9
U 54- 1	high
U 54- 2	UU48
U 54- 3	UU48
U 54- 4	9F01
U 54- 5	C4AH
U 54- 6	CP5H
U 54- 7	4HF8
U 54- 9	37U6
U 54-10	267A
U 54-11	7U03
U 54-12	UU48
U 54-13	low
U 54-14	UU48
U 54-15	3U7P
U 55- 1	high
U 55- 2	69C9
U 55- 4	6P70
U 55- 6	low
U 55- 7	low
U 55- 9	3U7P
U 55-10	low
U 55-11	71P0
U 55-12	U7F0
U 55-13	14U6
U 55-15	low
U 67- 1	high
U 67- 2	U7F0
U 67- 3	low
U 67- 5	37U6
U 67- 6	2UUC
U 67- 7	37U6
U 67- 9	37U6
U 67-10	U7F0
U 67-11	1UAF
U 67-12	37U6
U 67-13	low
U 67-14	HU9A
U 71- 1	high
U 71- 2	1UAF
U 71- 3	2UUC
U 71- 4	53HC
U 71- 5	7U03
U 71- 6	1UAF
U 71- 7	2UUC
U 71-10	53HC
U 71-11	29PH
U 71-12	14U6
U 71-13	29PH
U 71-14	14U6
U 71-15	6P70
U 73- 1	high
U 73- 2	FFU8
U 73- 3	8277
U 73- 4	P116
U 73- 5	7205
U 73- 6	FFU8
U 73- 7	8277
U 73-10	P116
U 73-11	C4AH
U 73-12	CP5H
U 73-13	C4AH
U 73-14	CP5H
U 73-15	7U03
U 86- 2	7205
U 86- 3	0000
U 86-12	37U6
U 86-14	89H1

64601A Timing Control Board
LESS THAN INTERVAL B #7

NORM MODE

VH = 593A

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Temporarily connect U13 pins 12 and 14 together

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 pos. edge
Location of GROUND: gnd

TTL

U 44- 1	high	U 47- 6	0.16 DCV	U 90-14	593A		
U 44- 2	low	U 47- 7	0.01 DCV	U 90-15	high		
U 44- 3	HHHU	U 47- 8	4.99 DCV	U 91- 1	0583		
U 44- 4	4UA2	U 47- 9	0.16 DCV	U 91- 2	CU50		
U 44- 5	low	U 47-10	0.01 DCV	U 91- 3	05C0		
U 44- 6	low	U 47-11	4.99 DCV	U 91- 4	593A		
U 44- 7	869F	U 47-12	0.91 DCV	U 91- 5	0000		
U 44- 8	5153	U 47-13	0.01 DCV	U 91- 6	high		
U 44- 9	low	U 47-14	0.04 DCV	U 91- 7	593A		
U 44-11	593A	U 49- 4	8F3U	U 91-12	593A		
U 44-12	high	U 49- 5	P7A2	U 91-13	593A		
U 44-13	8067	U 49-12	low	U 91-14	high		
U 44-14	3F17	U 49-13	F8C7	U 91-15	593A		
U 44-15	low	U 85- 1	593A				
U 44-16	high	U 85- 2	8F3U				
U 44-18	8874	U 85- 3	822P				
U 44-19	low	U 85- 4	P7A2				
U 46- 1	-4.53 DCV	U 85- 5	A9A6				
U 46- 2	-5.17 DCV	U 85- 6	9226				
U 46- 3	-5.11 DCV	U 85- 7	FPA8				
U 46- 4	-5.17 DCV	U 85- 9	H6H5				
U 46- 5	-4.36 DCV	U 85-12	7020				
U 46- 6	-4.89 DCV	U 85-14	H780				
U 46- 7	-5.17 DCV	U 85-15	P5AF				
U 46- 8	-5.17 DCV	U 85-16	C197				
U 46- 9	-0.81 DCV	U 85-17	low				
U 46-10	0.16 DCV	U 85-18	A9A8				
U 46-11	0.01 DCV	U 85-19	593A				
U 46-12	-5.17 DCV	U 86- 5	H14P				
U 46-13	0.64 DCV	U 86- 7	593A				
U 46-14	0.01 DCV	U 86-10	9266				
U 46-15	-4.36 DCV	U 86-11	P5AF				
U 46-16	-4.53 DCV	U 90- 1	74F9				
U 47- 1	4.99 DCV	U 90- 2	06HC				
U 47- 2	0.16 DCV	U 90- 3	292H				
U 47- 3	0.01 DCV	U 90- 4	low				
U 47- 4	0.16 DCV	U 90- 5	9266				
U 47- 5	4.99 DCV	U 90- 6	P5AF				

ECL

U 5- 2	~ 24 MHz	U 35-13	074F	U 42-12	0U33
U 5- 3	~ 24 MHz	U 35-15	18H4	U 43- 1	high
U 7- 2	~ 24 MHz	U 36- 1	0000	U 43- 2	high
U 7- 3	~ 24 MHz	U 36- 3	224A	U 43- 4	0U33
U 10- 1	high	U 36- 4	8F3U	U 43- 5	low
U 10- 2	F19U	U 36- 6	high	U 43- 7	5831
U 10- 3	3U67	U 36- 7	low	U 43- 9	high
U 10- 4	9UC3	U 36- 9	P7A2	U 43-10	low
U 10- 5	6870	U 36-10	8F3U	U 43-11	18H4
U 10- 6	F19U	U 36-12	0000	U 43-12	18H4
U 10- 7	3U67	U 36-13	FC5F	U 43-13	41PP
U 10-10	9UC3	U 36-14	0000	U 43-14	41PP
U 10-11	P5H6	U 36-15	high	U 49- 3	8F3U
U 10-12	074F	U 36-17	0000	U 49- 7	P7A2
U 10-13	P5H6	U 36-18	low	U 49-11	low
U 10-14	074F	U 36-19	high	U 49-15	F8C7
U 10-15	HF0P	U 36-20	high	U 54- 1	high
U 15- 1	high	U 36-24	FC5F	U 54- 2	AH52
U 15- 2	0U33	U 37- 1	0000	U 54- 3	AH52
U 15- 3	5831	U 37- 3	848H	U 54- 4	2U82
U 15- 4	8617	U 37- 4	116F	U 54- 5	1941
U 15- 5	U528	U 37- 6	high	U 54- 6	A6AU
U 15- 6	0U33	U 37- 7	low	U 54- 7	PF6H
U 15- 7	5831	U 37- 9	F8C7	U 54- 9	FC5F
U 15-10	8617	U 37-10	low	U 54-10	1817
U 15-11	C6AF	U 37-12	0000	U 54-11	26U0
U 15-12	84UP	U 37-13	FC5F	U 54-12	AH52
U 15-13	C6AF	U 37-14	0000	U 54-13	low
U 15-14	84UP	U 37-15	high	U 54-14	AH52
U 15-15	6870	U 37-17	0000	U 54-15	U468
U 17- 1	high	U 37-18	low	U 55- 1	high
U 17- 2	46A2	U 37-19	high	U 55- 2	F8C7
U 17- 3	1U98	U 37-20	high	U 55- 4	A33H
U 17- 4	8617	U 37-24	FC5F	U 55- 6	low
U 17- 5	low	U 38- 1	0000	U 55- 7	low
U 17- 6	low	U 38- 3	HF0P	U 55- 9	U468
U 17- 7	C6AF	U 38- 4	848H	U 55-10	low
U 17- 9	low	U 38- 6	high	U 55-11	116F
U 17-10	low	U 38- 7	low	U 55-12	P7A2
U 17-11	84UP	U 38- 9	high	U 55-13	1264
U 17-12	0000	U 38-10	2U82	U 55-15	low
U 17-13	6870	U 38-12	0000	U 67- 1	high
U 17-14	0000	U 38-13	FC5F	U 67- 2	low
U 17-15	low	U 38-14	0000	U 67- 3	low
U 34- 1	high	U 38-15	high	U 67- 5	FC5F
U 34- 6	90AP	U 38-17	0000	U 67- 6	06F8
U 34-13	074F	U 38-18	low	U 67- 7	CP98
U 34-14	5P76	U 38-19	high	U 67- 9	FC5F
U 34-15	high	U 38-20	high	U 67-10	P7A2
U 35-10	5P76	U 38-24	FC5F	U 67-11	P6HU
U 35-11	46A2	U 42- 9	low	U 67-12	FC5F
U 35-12	1U98	U 42-10	high	U 67-13	low

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U 67-14  CUP5
U 67-15  593A
U 71- 1  high
U 71- 2  P6HU
U 71- 3  06F8
U 71- 4  U6F3
U 71- 5  26U0
U 71- 6  P6HU
U 71- 7  06F8
U 71- 9  0000
U 71-10  U6F3
U 71-11  24F9
U 71-12  1264
U 71-13  24F9
U 71-14  1264
U 71-15  A33H
U 73- 1  high
U 73- 2  C5FP
U 73- 3  U0P8
U 73- 4  8HH3
U 73- 5  H14P
U 73- 6  C5FP
U 73- 7  U0P8
U 73- 9  0000
U 73-10  8HH3
U 73-11  1941
U 73-12  A6AU
U 73-13  1941
U 73-14  A6AU
U 73-15  26U0
U 86- 2  H14P
U 86- 3  0000
U 86-12  FC5F
U 86-14  FC1F
```

64601A Timing Control Board
TRANSITION TRIGGER B #8

NORM MODE

VH = FC27

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Temporarily connect U13 pins 12 and 14 together

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 pos. edge
Location of GROUND: gnd

TTL

U 49- 4	7P9C
U 49- 5	3242
U 49-12	low
U 49-13	H916
U 85- 1	FC27
U 85- 2	7P9C
U 85- 3	CU8A
U 85- 4	3242
U 85- 5	FAAC
U 85- 6	3244
U 85- 7	86PC
U 85- 9	2H80
U 85-12	0P04
U 85-14	HAU0
U 85-15	7FC5
U 85-16	1632
U 85-17	low
U 85-18	5535
U 85-19	FC27
U 86- 5	5C83
U 86- 7	FC27
U 86-10	324F
U 86-11	7FC5
U 90- 1	4P99
U 90- 2	F0HA
U 90- 3	4524
U 90- 4	low
U 90- 5	324F
U 90- 6	7FC5
U 90-12	high
U 90-13	H458
U 90-14	FC27
(TOTLZ=0001)	
U 90-15	high
U 91- 1	A0C0
U 91- 2	C7PA
U 91- 3	A0C7
U 91- 4	FC27
(TOTLZ=0207)	
U 91- 5	0000
(TOTLZ=0001)	
U 91- 6	high
U 91- 7	FC27
(TOTLZ=0001)	
U 91- 9	high
U 91-10	high
U 91-11	high
U 91-12	FC27
U 91-13	FC27
U 91-14	high
U 91-15	FC27

ECL

U 7- 1	high
U 7- 2	3242
U 7- 3	U965
U 7- 4	3242
U 7- 5	U965
U 7- 9	3242
U 7-10	U965
U 7-12	3242
U 7-13	U965
U 7-15	U965
U 10- 1	high
U 10- 2	P65A
U 10- 3	U32H
U 10- 4	8FH7
U 10- 5	7C5P
U 10- 6	P65A
U 10- 7	U32H
U 10- 9	0000
U 10-10	8FH7
U 10-11	9H9P
U 10-12	3C8P
U 10-13	9H9P
U 10-14	3C8P
U 10-15	4632
U 15- 1	high
U 15- 2	PPC6
U 15- 3	H9PU
U 15- 4	4243
U 15- 5	8004
U 15- 6	PPC6
U 15- 7	H9PU
U 15-10	4243
U 15-11	8U95
U 15-12	1F3U
U 15-13	8U95
U 15-14	1F3U
U 15-15	7C5P
U 17- 1	high

U 17- 2	PA12
U 17- 3	2135
U 17- 4	4243
U 17- 5	low
U 17- 6	low
U 17- 7	8U95
U 17- 9	low
U 17-10	low
U 17-11	1F3U
U 17-12	0002
U 17-13	7C5P
U 17-14	0002
U 17-15	low
U 34- 6	H19F
U 34- 7	1ACC
U 34- 9	H19F
U 34-13	3C8P
U 34-14	U0A9
U 34-15	FC27
U 35-10	U0A9
U 35-11	PA12
U 35-12	2135
U 35-13	3C8P
U 35-14	H19F
U 35-15	1ACC
U 36- 1	0000
U 36- 3	CC7P
U 36- 4	7P9C
U 36- 6	high
U 36- 7	low
U 36- 9	3242
U 36-10	7P9C
U 36-12	0000
U 36-13	U96C
U 36-14	0000
U 36-15	high
U 36-17	0000
U 36-18	low
U 36-19	high
U 36-20	high
U 36-24	U96C
U 37- 1	0000
U 37- 3	A38H
U 37- 4	U13P
U 37- 6	high
U 37- 7	low
U 37- 8	CU57
U 37- 9	H916
U 37-10	low
U 37-12	0000
U 37-13	U96C
U 37-14	0000
U 37-15	high
U 37-17	0000
U 37-18	low
U 37-19	high
U 37-20	high
U 37-24	U96C
U 38- 1	0000
U 38- 3	4632
U 38- 4	A38H
U 38- 6	high
U 38- 7	low
U 38- 9	high
U 38-10	P5U0
U 38-12	0000
U 38-13	U96C
U 38-14	0000
U 38-15	high
U 38-17	0000
U 38-18	low
U 38-19	high
U 38-20	high
U 38-24	U96C
U 42-10	FC27
U 42-11	1935
U 42-12	PPC6
U 42-13	H19F
U 42-14	CAF1
U 42-15	71P6
U 43- 1	high
U 43- 2	FC27
U 43- 3	1935
U 43- 4	PPC6
U 43- 5	low
U 43- 6	H19F
U 43- 7	H9PU
U 43- 9	FC27
U 43-10	low
U 43-11	1ACC
U 43-12	1ACC
U 43-13	H19F
U 43-14	H19F
U 43-15	0000
U 49- 3	7P9C
U 49- 7	3242
U 49-11	low
U 49-15	H916
U 54- 1	high
U 54- 2	8P72
U 54- 3	8P72
U 54- 4	P5U0
U 54- 5	3532
U 54- 6	PUH8
U 54- 7	H655
U 54- 9	U96C
U 54-10	7643
U 54-11	H958
U 54-12	8P72
U 54-13	low
U 54-14	8P72
U 54-15	4555
U 55- 1	high
U 55- 2	H916
U 55- 4	5691
U 55- 5	0580
U 55- 6	low
U 55- 7	low
U 55- 9	4555
U 55-10	low
U 55-11	U13P
U 55-12	3242
U 55-13	47A0
U 55-14	CAF1
U 55-15	low
U 67- 1	high
U 67- 2	low
U 67- 3	low
U 67- 4	71P6
U 67- 5	U96C
U 67- 6	0UC8
U 67- 7	U965
U 67- 9	U96C
U 67-10	3242
U 67-11	4218
U 67-12	U96C
U 67-13	low
U 67-14	893U
U 67-15	FC27
U 71- 1	high
U 71- 2	4218
U 71- 3	0UC8
U 71- 4	A968
U 71- 5	H958
U 71- 6	4218
U 71- 7	0UC8
U 71- 9	0000
U 71-10	A968
U 71-11	8U41
U 71-12	47A0
U 71-13	8U41
U 71-14	47A0
U 71-15	5691
U 73- 1	high
U 73- 2	266F
U 73- 3	P677
U 73- 4	HH8U
U 73- 5	5C83
U 73- 6	266F
U 73- 7	P677
U 73- 9	0000
U 73-10	HH8U

U 73-11 3532
U 73-12 PUH8
U 73-13 3532
U 73-14 PUH8
U 73-15 H958
U 86- 2 5C83
U 86- 3 0000
U 86-12 U96C
U 86-14 U963

64601A Timing Control Board
DISPLAY DRIVER #9

NORM MODE VH = 923F

DATA THRESHOLD HIGH: ttl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 pos. edge
Location of GROUND: gnd

TTL

U 56- 1 high	U 58- 8 923F	U 62- 9 P8UF
U 56- 2 high	(TOTLZ=32768)	U 62-10 high
U 56- 3 0C92	U 58-10 F995	U 62-11 P8UF
U 56- 4 U204	U 58-11 5351	U 62-12 4319
U 56- 5 622A	U 58-12 A545	U 62-14 4319
U 56- 6 6731	U 58-13 1A8H	U 62-15 low
U 56- 9 923F	U 58-14 HCHC	U 63- 1 4319
(TOTLZ=0048)	U 58-15 682U	U 63- 3 0000
U 56-10 low	U 58-16 6P3C	(TOTLZ=0FLO)
U 56-11 23HP	U 58-17 94AF	U 63- 4 H125
U 56-12 F24C	U 59- 1 416C	U 63- 5 4319
U 56-13 C443	U 59- 2 09AP	U 63- 6 H125
U 56-14 1C09	U 59- 3 2U5C	U 63- 8 high
U 56-15 4319	U 59- 4 F19H	U 63- 9 low
U 57- 1 416C	U 59- 5 9UPC	U 63-10 high
U 57- 2 09AP	U 59- 6 2C32	U 63-11 0000
U 57- 3 2U5C	U 59- 7 218A	(TOTLZ=0FLO)
U 57- 4 F19H	U 59- 8 923F	U 63-12 high
U 57- 5 9UPC	(TOTLZ=32768)	U 63-13 low
U 57- 6 2C32	U 59-10 4FAH	U 76- 1 923F
U 57- 7 39C2	U 59-11 C883	(TOTLZ=32764)
U 57- 8 923F	U 59-12 A545	U 76- 2 39C2
(TOTLZ=32768)	U 59-13 1A8H	U 76- 3 93P7
U 57-10 2656	U 59-14 HCHC	U 76- 4 2490
U 57-11 93P7	U 59-15 682U	U 76- 5 5351
U 57-12 A545	U 59-16 6P3C	U 76- 6 218A
U 57-13 1A8H	U 59-17 94AF	U 76- 7 C883
U 57-14 HCHC	U 62- 1 low	U 76- 9 AA8F
U 57-15 682U	U 62- 2 923F	U 76-10 2UCH
U 57-16 6P3C	(TOTLZ=65552)	U 76-11 C252
U 57-17 94AF	U 62- 3 low	U 76-12 C078
U 58- 1 416C	U 62- 4 923F	U 76-13 4HCC
U 58- 2 09AP	(TOTLZ=65552)	U 76-14 5C60
U 58- 3 2U5C	U 62- 5 923F	U 76-15 923F
U 58- 4 F19H	(TOTLZ=65552)	(TOTLZ=32764)
U 58- 5 9UPC	U 62- 6 4319	U 77- 1 F19H
U 58- 6 2C32	U 62- 7 923F	U 77- 2 2U5C
U 58- 7 2490	(TOTLZ=65552)	U 77- 3 09AP

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U 77- 4  416C
U 77- 5  2C32
U 77- 6  94AF
U 77- 7  6P3C
U 77- 8  low
U 77- 9  4HCC
U 77-10  5C60
U 77-11  AA8F
U 77-12  2UCH
U 77-15  C252
U 77-16  C078
U 77-17  high
U 77-18  low
U 77-19  9925
U 77-20  923F
(TOTLZ=0018)
U 77-21  9UPC
U 77-22  high
U 81- 1  low
U 81- 2  low
U 81- 3  5C60
U 81- 4  low
U 81- 5  low
U 81- 6  C078
U 81- 7  low
U 81- 9  low
U 81-10  low
U 81-11  low
U 81-12  low
U 81-13  low
U 81-14  high
U 81-15  low
U 82- 1  0000
(TOTLZ=65552)
U 82- 2  F24C
U 82- 3  923F
(TOTLZ=32768)
U 82- 4  0000
(TOTLZ=65552)
U 82- 5  0000
(TOTLZ=65552)
U 82- 6  923F
(TOTLZ=65552)
U 82- 8  H125
U 82- 9  high
U 82-10  4319
U 82-11  high
U 82-12  low
U 82-13  low
U 85- 1  high
U 85- 2  low
U 85- 3  U204
U 85- 4  low
U 85- 5  0C92
U 85- 6  high
U 85- 7  C252
U 85- 8  low
U 85- 9  4HCC
U 85-12  AA8F
U 85-14  C883
U 85-15  low
U 85-16  5351
U 85-17  low
U 85-18  93P7
U 85-19  high
U 88- 1  low
U 88- 2  high
U 88- 3  0000
(TOTLZ=99213)
U 88- 4  0000
(TOTLZ=98537)
U 88- 5  923F
(TOTLZ=OFLO)
U 88- 6  0000
(TOTLZ=99213)
U 88- 8  low
U 88- 9  high
U 88-10  low
U 88-11  high
U 88-12  high
U 88-13  low
U 90- 1  2H31
U 90- 2  A279
U 90- 3  3952
U 90- 4  low
U 90- 5  high
U 90- 6  low
U 90- 7  9925
U 90- 9  2656
U 90-10  F995
U 90-11  4FAH
U 90-12  high
U 90-13  0840
U 90-14  923F
(TOTLZ=0133)
U 90-15  high
U 91- 1  5A58
U 91- 2  7UP0
U 91- 3  0P2F
U 91- 4  923F
(TOTLZ=OFLO)
U 91- 5  0000
(TOTLZ=99213)
U 91- 6  high
U 91- 7  923F
(TOTLZ=0133)
U 91- 9  923F
(TOTLZ=32764)
U 91-10  923F
(TOTLZ=0048)
U 91-11  923F
(TOTLZ=65552)
U 91-12  high
U 91-13  high
U 91-14  923F
(TOTLZ=0040)
U 91-15  high
U 92- 1  high
U 92- 2  CCHU
U 92- 3  93P7
U 92- 4  5351
U 92- 5  F265
U 92- 6  C883
U 92- 7  248F
U 92- 9  923F
(TOTLZ=0040)
U 92-10  CU28
U 92-11  AA8F
U 92-12  H1CA
U 92-13  4HCC
U 92-14  C252
U 92-15  6CU1
U 93- 1  high
U 93- 2  82HU
U 93- 3  0C92
U 93- 4  U204
U 93- 5  2665
U 93- 6  6731
U 93- 7  C48P
U 93- 9  923F
(TOTLZ=0040)
U 93-10  UU22
U 93-11  23HP
U 93-12  H193
U 93-13  C443
U 93-14  1C09
U 93-15  6C54
U 94- 1  high
U 94- 2  923F
(TOTLZ=65552)
U 94- 3  CCHU
U 94- 4  F265
U 94- 5  248F
U 94- 6  CU28
U 94- 7  high
U 94- 9  4319
U 94-10  high
U 94-11  F19H
U 94-12  2U5C
U 94-13  09AP
U 94-14  416C
U 94-15  HPU4
```

```
U 95- 1  high
U 95- 2  923F
(TOTLZ=65552)
U 95- 3  H1CA
U 95- 4  6CU1
U 95- 5  82HU
U 95- 6  2665
U 95- 7  high
U 95- 9  4319
U 95-10  HPU4
U 95-11  6P3C
U 95-12  94AF
U 95-13  2C32
U 95-14  9UPC
U 95-15  P8UF
U 96- 1  high
U 96- 2  923F
(TOTLZ=65552)
U 96- 3  C48P
U 96- 4  UU22
U 96- 5  H193
U 96- 6  6C54
U 96- 7  high
U 96- 9  4319
U 96-10  P8UF
U 96-11  A545
U 96-12  1A8H
U 96-13  HCHC
U 96-14  682U
U 96-15  89HF
```

64601A Timing Control Board
RATES / INTERVAL A #10

NORM MODE VH = F036

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 pos. edge
Location of GROUND: gnd

TTL

U 28- 1	high
U 28- 2	4999
U 28- 3	H18U
U 28- 4	CCU5
U 28- 5	159C
U 28- 6	3P42
U 28- 7	6FCU
U 28- 8	4A31
U 28- 9	0HFA
U 28-11	F036
U 28-12	AUCF
U 28-13	5P4A
U 28-14	U1C5
U 28-15	3P30
U 28-16	3078
U 28-17	U5PH
U 28-18	0P0P
U 28-19	low
U 49- 4	29C4
U 49- 5	U7F0
U 49-12	low
U 49-13	PH4P
U 85- 1	F036
U 85- 2	29C4
U 85- 3	0P0P
U 85- 4	U7F0
U 85- 5	U5PH
U 85- 6	low
U 85- 7	U1C5
U 85- 9	5P4A
U 85-12	4A31
U 85-14	6FCU
U 85-15	5FA5
U 85-16	CCU5
U 85-17	low
U 85-18	H18U
U 85-19	F036
U 86- 5	329A
U 86- 7	F036
U 86-10	U7F0
U 86-11	5FA5
U 90- 1	2F7F
U 90- 2	6914
U 90- 3	7466
U 90- 4	low
U 90- 5	U7F0
U 90- 6	5FA5
U 90-13	C3A7
U 90-14	F036
(TOTLZ=0001)	
U 90-15	high
U 91- 1	63C9
U 91- 2	884H
U 91- 3	947H
U 91- 4	F036
(TOTLZ=0207)	
U 91- 5	0000
(TOTLZ=0002)	
U 91- 6	high
U 91- 7	F036
(TOTLZ=0001)	
U 91- 9	high
U 91-10	high
U 91-11	high
U 91-12	F036
U 91-13	F036
U 91-14	high
U 91-15	F036

ECL

U 7- 1	high
U 7- 2	49P7
U 7- 3	89H1
U 7- 4	49P7
U 7- 5	89H1
U 7- 6	49P7
U 7- 7	89H1
U 7- 9	49P7
U 7-10	89H1
U 7-12	49P7
U 7-13	89H1
U 7-15	89H1
U 10- 1	high
U 10- 2	64P5
U 10- 3	1F57
U 10- 4	4U8C
U 10- 5	141P
U 10- 6	64P5
U 10- 7	1F57
U 10- 9	0000
U 10-10	4U8C
U 10-11	63P3
U 10-12	U4C8
U 10-13	63P3
U 10-14	U4C8
U 10-15	CP7A
U 11- 1	high
U 11- 2	3AUP
U 11- 3	9H7U
U 11- 4	2AC4
U 11- 5	75UF
U 11- 6	3AUP
U 11- 7	9H7U
U 11- 9	0000
U 11-10	2AC4
U 11-11	C577
U 11-12	9P9H
U 11-13	C577

U 11-14	9P9H
U 11-15	2C45
U 13- 1	high
U 13- 2	8H5H
U 13- 3	4H6C
U 13- 4	2AC4
U 13- 5	low
U 13- 6	low
U 13- 7	C577
U 13- 9	low
U 13-10	U7F0
U 13-11	9P9H
U 13-12	0000
U 13-13	2C45
U 13-14	high
U 13-15	low
U 27- 1	high
U 27- 2	high
U 27- 4	3AUP
U 27- 5	low
U 27- 7	9H7U
U 27- 9	high
U 27-10	low
U 27-11	C9H3
U 27-12	C9H3
U 27-13	79P5
U 27-14	79P5
U 27-15	0000
U 34- 1	high
U 34-13	U4C8
U 34-14	348P
U 34-15	F036
U 35- 1	high
U 35- 2	C9H3
U 35- 4	348P
U 35- 5	8H5H
U 35- 6	4H6C
U 35- 7	U4C8
U 36- 1	0000
U 36- 3	9FF8
U 36- 6	high
U 36- 7	low
U 36- 9	49P7
U 36-12	0000
U 36-13	37U6
U 36-14	0000
U 36-15	high
U 36-17	0000
U 36-18	low
U 36-19	high
U 36-20	high
U 36-24	37U6
U 37- 1	0000
U 37- 3	F8H1
U 37- 4	5UA9
U 37- 6	high
U 37- 7	low
U 37- 8	37AC
U 37- 9	PH4P
U 37-10	U7F0
U 37-12	0000
U 37-13	37U6
U 37-14	0000
U 37-15	high
U 37-17	0000
U 37-18	low
U 37-19	high
U 37-20	high
U 37-24	37U6
U 38- 1	0000
U 38- 3	CP7A
U 38- 4	F8H1
U 38- 6	high
U 38- 7	low
U 38- 9	high
U 38-10	9F01
U 38-12	0000
U 38-13	37U6
U 38-14	0000
U 38-15	high
U 38-17	0000
U 38-18	low
U 38-19	high
U 38-20	high
U 38-24	37U6
U 42- 1	high
U 42- 2	F036
U 42- 4	high
U 42- 6	3AUP
U 49- 7	U7F0
U 49-11	low
U 49-15	PH4P
U 54- 1	high
U 54- 2	F746
U 54- 3	F746
U 54- 4	9F01
U 54- 5	10A4
U 54- 6	6F59
U 54- 7	6C58
U 54- 9	37U6
U 54-10	5667
U 54-11	1601
U 54-12	F746
U 54-13	low
U 54-14	F746
U 54-15	0770
U 55- 1	high
U 55- 2	PH4P
U 55- 4	75UF
U 55- 6	low
U 55- 7	low
U 55- 9	0770
U 55-10	low
U 55-11	5UA9
U 55-12	U7F0
U 55-13	63C5
U 55-15	low
U 67- 1	high
U 67- 2	U7F0
U 67- 3	low
U 67- 5	37U6
U 67- 6	C5CC
U 67- 7	37U6
U 67- 9	37U6
U 67-10	U7F0
U 67-11	2C2H
U 67-12	37U6
U 67-13	low
U 67-14	PC1C
U 71- 1	high
U 71- 2	2C2H
U 71- 3	C5CC
U 71- 4	1PUC
U 71- 5	1601
U 71- 6	2C2H
U 71- 7	C5CC
U 71- 9	0000
U 71-10	1PUC
U 71-11	0U7H
U 71-12	63C5
U 71-13	0U7H
U 71-14	63C5
U 71-15	75UF
U 73- 1	high
U 73- 2	PFC7
U 73- 3	1250
U 73- 4	A905
U 73- 5	329A
U 73- 6	PFC7
U 73- 7	1250
U 73- 9	0000
U 73-10	A905
U 73-11	10A4
U 73-12	6F59
U 73-13	10A4
U 73-14	6F59
U 73-15	1601
U 86- 2	329A
U 86- 3	0000
U 86-12	37U6
U 86-13	F036

64601A Timing Control Board
LESS THAN INTERVAL A # 11

NORM MODE VH = 593A

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 pos. edge
Location of GROUND: gnd

TTL

U 28- 1	high	U 31- 1	-4.53 DCV	U 32- 5	4.98 DCV	U 85- 1	593A
U 28- 2	low	U 31- 2	-5.17 DCV	U 32- 6	0.17 DCV	U 85- 2	U7F2
U 28- 3	A9A8	U 31- 3	-5.1 DCV	U 32- 7	0.01 DCV	U 85- 3	822P
U 28- 4	C197	U 31- 4	-5.17 DCV	U 32- 8	4.98 DCV	U 85- 4	P7A2
U 28- 5	low	U 31- 5	-4.37 DCV	U 32- 9	0.16 DCV	U 85- 5	A9A6
U 28- 6	low	U 31- 6	-4.94 DCV	U 32-10	0.01 DCV	U 85- 6	9226
U 28- 7	H780	U 31- 7	-5.17 DCV	U 32-11	4.98 DCV	U 85- 7	FPA8
U 28- 8	7020	U 31- 8	-5.17 DCV	U 32-12	0.91 DCV	U 85- 9	H6H5
U 28- 9	low	U 31- 9	-0.83 DCV	U 32-13	0.01 DCV	U 85-12	7020
U 28-11	593A	U 31-10	0.16 DCV	U 32-14	0.03 DCV	U 85-14	H780
U 28-12	high	U 31-11	0.01 DCV	U 49- 4	U7F2	U 85-15	P5AF
U 28-13	H6H5	U 31-12	-5.17 DCV	U 49- 5	P7A2	U 85-16	C197
U 28-14	FPA8	U 31-13	0.64 DCV	U 49-12	low	U 85-17	low
U 28-15	low	U 31-14	0.01 DCV	U 49-13	F8C7	U 85-18	A9A8
U 28-16	high	U 31-15	-4.37 DCV			U 85-19	593A
U 28-17	A9A6	U 31-16	-4.52 DCV			U 86- 5	AAC3
U 28-18	822P	U 32- 1	4.98 DCV			U 86- 7	593A
U 28-19	low	U 32- 2	0.17 DCV			U 86-10	9266
		U 32- 3	0.01 DCV			U 86-11	P5AF
		U 32- 4	0.17 DCV			U 90- 1	74F9
						U 90- 2	06HC
						U 90- 3	292H
						U 90- 4	low
						U 90- 5	9266
						U 90- 6	P5AF
						U 90-14	593A
						U 90-15	high
						U 91- 1	0583
						U 91- 2	CU50
						U 91- 3	05C0
						U 91- 4	593A
						(TOTLZ=0207)	
						U 91- 5	0000
						(TOTLZ=0002)	
						U 91- 6	high
						U 91- 7	593A
						(TOTLZ=0001)	
						U 91-12	593A
						U 91-13	593A
						U 91-15	593A

ECL

U 10- 1	high
U 10- 2	HC17
U 10- 3	C223
U 10- 4	H911
U 10- 5	5H61
U 10- 6	HC17
U 10- 7	C223
U 10- 9	0000
U 10-10	H911
U 10-11	F687
U 10-12	16P4
U 10-13	F687
U 10-14	16P4
U 10-15	H4HA
U 11- 1	high
U 11- 2	2A42
U 11- 3	FA89
U 11- 4	4U4C
U 11- 5	009A
U 11- 6	2A42
U 11- 7	FA89
U 11- 9	0000
U 11-10	4U4C
U 11-11	H202
U 11-12	36A9
U 11-13	H202
U 11-14	36A9
U 11-15	C15C
U 13- 1	high
U 13- 2	3699
U 13- 3	6UA3
U 13- 4	4U4C
U 13- 5	low
U 13- 6	low
U 13- 7	H202
U 13- 9	low
U 13-10	low
U 13-11	36A9
U 13-12	0000
U 13-13	C15C
U 13-14	high
U 13-15	low
U 27- 1	high
U 27- 2	high
U 27- 4	2A42
U 27- 5	low
U 27- 7	FA89
U 27- 9	high
U 27-10	low
U 27-11	7947
U 27-12	7947
U 27-13	207H
U 27-14	207H
U 27-15	0000
U 34- 1	high
U 34- 2	7P7F
U 34- 6	0915
U 34-13	16P4
U 34-14	4UHP
U 36- 1	0000
U 36- 3	A5AF
U 36- 6	high
U 36- 7	low
U 36- 9	P7A2
U 36-12	0000
U 36-13	FC5F
U 36-14	0000
U 36-15	high
U 36-17	0000
U 36-18	low
U 36-19	high
U 36-20	high
U 36-24	FC5F
U 37- 1	0000
U 37- 3	1H36
U 37- 4	HPU6
U 37- 6	high
U 37- 7	low
U 37- 9	F8C7
U 37-10	0000
U 37-12	0000
U 37-13	FC5F
U 37-14	0000
U 37-15	high
U 37-17	0000
U 37-18	low
U 37-19	high
U 37-20	high
U 37-24	FC5F
U 38- 1	0000
U 38- 3	H4HA
U 38- 4	1H36
U 38- 6	high
U 38- 7	low
U 38- 9	high
U 38-10	2U82
U 38-12	0000
U 38-13	FC5F
U 38-14	0000
U 38-15	high
U 38-17	0000
U 38-18	low
U 38-19	high
U 38-20	high
U 38-24	FC5F
U 42- 1	high
U 42- 2	593A
U 42- 4	593A
U 42- 5	AC7U
U 42- 6	2A42
U 49- 7	P7A2
U 49-11	low
U 49-15	F8C7
U 54- 1	high
U 54- 2	P8HH
U 54- 3	P8HH
U 54- 4	2U82
U 54- 5	1PUP
U 54- 6	2570
U 54- 7	P073
U 54- 9	FC5F
U 54-10	1242
U 54-11	P71U
U 54-12	P8HH
U 54-13	low
U 54-14	P8HH
U 54-15	C1P7
U 55- 1	high
U 55- 2	F8C7
U 55- 4	009A
U 55- 5	3U34
U 55- 6	low
U 55- 7	low
U 55- 9	C1P7
U 55-10	low
U 55-11	HPU6
U 55-12	P7A2
U 55-13	CP64
U 55-15	low
U 67- 1	high
U 67- 2	low
U 67- 3	low
U 67- 5	FC5F
U 67- 6	36C3
U 67- 7	CP98
U 67- 9	FC5F
U 67-10	P7A2
U 67-11	8628
U 67-12	FC5F
U 67-13	low
U 67-14	HU12
U 67-15	593A
U 71- 1	high
U 71- 2	8628
U 71- 3	36C3
U 71- 4	PPUP

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U 71- 5  P71U
U 71- 6  8628
U 71- 7  36C3
U 71- 9  0000
U 71-10  PPUP
U 71-11  28H7
U 71-12  CP64
U 71-13  28H7
U 71-14  CP64
U 71-15  009A
U 73- 1  high
U 73- 2  8830
U 73- 3  PP17
U 73- 4  82AF
U 73- 5  AAC3
U 73- 6  8830
U 73- 7  PP17
U 73- 9  0000
U 73-10  82AF
U 73-11  1PUP
U 73-12  2570
U 73-13  1PUP
U 73-14  2570
U 73-15  P71U
U 86- 2  AAC3
U 86- 3  0000
U 86-12  FC5F
U 86-14  FC1F
```

64601A Timing Control Board
TRANSITION TRIGGER A #12

NORM MODE VH = FC27

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 pos. edge
Location of GROUND: gnd

TTL

U 49- 4	71P4
U 49- 5	3242
U 49-12	low
U 49-13	H916
U 85- 1	FC27
U 85- 2	71P4
U 85- 3	CU8A
U 85- 4	3242
U 85- 5	FAAC
U 85- 6	3244
U 85- 7	86PC
U 85- 9	2H80
U 85-12	0P04
U 85-14	HAU0
U 85-15	7FC5
U 85-16	1632
U 85-17	low
U 85-18	5535
U 85-19	FC27
U 86- 5	54UF
U 86- 7	FC27
U 86-10	324F
U 86-11	7FC5
U 90- 1	4P99
U 90- 2	F0HA
U 90- 3	4524
U 90- 4	low
U 90- 5	324F
U 90- 6	7FC5
U 90-13	FAA7
U 90-14	FC27
(TOTLZ=0001)	
U 90-15	high
U 91- 1	A0C0
U 91- 2	C7PA
U 91- 3	A0C7
U 91- 4	FC27
(TOTLZ=0207)	
U 91- 5	0000
(TOTLZ=0002)	
U 91- 6	high
U 91- 7	FC27
(TOTLZ=0001)	
U 91- 9	high
U 91-10	high
U 91-11	high
U 91-12	FC27
U 91-13	FC27
U 91-14	high
U 91-15	FC27

ECL

U 7- 1	high
U 7- 2	3242
U 7- 3	U965
U 7- 4	3242
U 7- 5	U965
U 7- 6	3242
U 7- 7	U965
U 7- 9	3242
U 7-10	U965
U 7-12	3242
U 7-13	U965
U 7-15	U965
U 10- 1	high
U 10- 2	F50C
U 10- 3	P285
U 10- 4	8403
U 10- 5	3HUF
U 10- 6	F50C
U 10- 7	P285
U 10- 9	0000
U 10-10	8403
U 10-11	19U4
U 10-12	79CC
U 10-13	19U4
U 10-14	79CC
U 10-15	6728
U 11- 1	high
U 11- 2	9433
U 11- 3	P4AH
U 11- 4	HFP2
U 11- 5	F2P5
U 11- 6	9433
U 11- 7	P4AH
U 11- 9	0000
U 11-10	HFP2
U 11-11	F0F5
U 11-12	CC97
U 11-13	F0F5

U 11-14	CC97
U 11-15	288A
U 13- 1	high
U 13- 2	9905
U 13- 3	5222
U 13- 4	HFP2
U 13- 5	low
U 13- 6	low
U 13- 7	F0F5
U 13- 9	low
U 13-10	low
U 13-11	CC97
U 13-12	0002
U 13-13	288A
U 13-14	high
U 13-15	low
U 27- 1	high
U 27- 2	high
U 27- 3	58C6
U 27- 4	9433
U 27- 5	low
U 27- 6	P0CP
U 27- 7	P4AH
U 27- 9	high
U 27-10	low
U 27-11	2C99
U 27-12	2C99
U 27-13	P0CP
U 27-14	P0CP
U 34- 1	high
U 34- 2	P0CP
U 34- 3	2C99
U 34- 4	P0CP
U 34-13	79CC
U 34-14	C29F
U 35- 1	high
U 35- 2	2C99
U 35- 3	P0CP
U 35- 4	C29F
U 35- 5	9905
U 35- 6	5222
U 35- 7	79CC
U 36- 1	0000
U 36- 3	PC82
U 36- 4	71P4
U 36- 6	high
U 36- 7	low
U 36- 9	3242
U 36-12	0000
U 36-13	U96C
U 36-14	0000
U 36-15	high
U 36-17	0000
U 36-18	low
U 36-19	high
U 36-20	high
U 36-24	U96C
U 37- 1	0000
U 37- 3	10CA
U 37- 4	28FH
U 37- 6	high
U 37- 7	low
U 37- 8	9P4H
U 37- 9	H916
U 37-10	0000
U 37-12	0000
U 37-13	U96C
U 37-14	0000
U 37-15	high
U 37-17	0000
U 37-18	low
U 37-19	high
U 37-20	high
U 37-24	U96C
U 38- 1	0000
U 38- 3	6728
U 38- 4	10CA
U 38- 6	high
U 38- 7	low
U 38- 9	high
U 38-10	P5U0
U 38-12	0000
U 38-13	U96C
U 38-14	0000
U 38-15	high
U 38-17	0000
U 38-18	low
U 38-19	high
U 38-20	high
U 38-24	U96C
U 42- 1	high
U 42- 2	high
U 42- 3	FU52
U 42- 4	FC27
U 42- 5	58C6
U 42- 6	9433
U 42- 7	P0CP
U 49- 7	3242
U 49-11	low
U 49-15	H916
U 54- 1	high
U 54- 2	F6F3
U 54- 3	F6F3
U 54- 4	P5U0
U 54- 5	55F5
U 54- 6	HUA3
U 54- 7	H7H6
U 54- 9	U96C
U 54-10	U709
U 54-11	F165
U 54-12	F6F3
U 54-13	low
U 54-14	F6F3
U 54-15	0HP4
U 55- 1	high
U 55- 2	H916
U 55- 4	F2P5
U 55- 5	FU52
U 55- 6	low
U 55- 7	low
U 55- 9	0HP4
U 55-10	low
U 55-11	28FH
U 55-12	3242
U 55-13	3220
U 55-14	768C
U 55-15	low
U 67- 1	high
U 67- 2	low
U 67- 3	low
U 67- 4	CHAF
U 67- 5	U96C
U 67- 6	09C7
U 67- 7	U965
U 67- 9	U96C
U 67-10	3242
U 67-11	4P06
U 67-12	U96C
U 67-13	low
U 67-14	8521
U 67-15	high
U 71- 1	high
U 71- 2	4P06
U 71- 3	09C7
U 71- 4	AA6U
U 71- 5	F165
U 71- 6	4P06
U 71- 7	09C7
U 71- 9	0000
U 71-10	AA6U
U 71-11	8PF2
U 71-12	3220
U 71-13	8PF2
U 71-14	3220
U 71-15	F2P5
U 73- 1	high
U 73- 2	21H3
U 73- 3	65A8
U 73- 4	1F60
U 73- 5	54UF
U 73- 6	21H3
U 73- 7	65A8

```
U 73- 9   0000
U 73-10   1F60
U 73-11   55F5
U 73-12   HUA3
U 73-13   55F5
U 73-14   HUA3
U 73-15   F165
U 86- 2   54UF
U 86- 3   0000
U 86-12   U96C
U 86-14   U963
```

64601A Timing Control Board
AND #13

NORM MODE VH = 60AU

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 pos. edge
Location of GROUND: gnd tp 7

TTL

U 49- 4	H830
U 49- 5	894F
U 49-12	low
U 49-13	HF59
U 64- 4	low
U 64- 5	P0H1
U 64-12	PU50
U 64-13	low
U 85- 1	60AU
(TOTLZ=0004)	
U 85- 2	H830
U 85- 3	H4CU
U 85- 4	894F
U 85- 5	6H5P
U 85- 6	low
U 85- 7	6HF7
U 85- 8	low
U 85- 9	55P2
U 85-11	PU50
U 85-12	2H1C
U 85-13	P0H1
U 85-14	HU32
U 85-15	6390
U 85-16	1278
U 85-17	low
U 85-18	05C6
U 85-19	60AU
(TOTLZ=0004)	

ECL

U 10- 1	high
U 10- 2	622H
U 10- 3	1696
U 10- 4	8C4C
U 10- 5	2AAA
U 10- 6	622H
U 10- 7	1696
U 10- 9	0000
(TOTLZ=0130)	
U 10-10	8C4C
U 10-11	32HH
U 10-12	4996
U 10-13	32HH
U 10-14	4996
U 10-15	834C
U 11- 1	high
U 11- 2	UHCP
U 11- 3	7PHU
U 11- 4	4817
U 11- 5	UC7H
U 11- 6	UHCP
U 11- 7	7PHU
U 11- 9	0000
(TOTLZ=0130)	
U 11-10	4817
U 11-11	U4U3
U 11-12	HHU9
U 11-13	U4U3
U 11-14	HHU9
U 11-15	PPUF
U 13- 1	high
U 13- 2	U781
U 13- 3	972P
U 13- 4	4817
U 13- 5	low
U 13- 6	low
U 13- 7	U4U3
U 13- 9	low
U 13-10	low
U 13-11	HHU9
U 13-12	4764
U 13-13	PPUF
U 13-14	1HP7
U 13-15	low
U 15- 1	high
U 15- 2	777P
U 15- 3	3CCU
U 15- 4	6AA7
U 15- 5	PPUF
U 15- 6	777P
U 15- 7	3CCU
U 15- 9	0000
(TOTLZ=0130)	
U 15-10	6AA7
U 15-11	P5AC
U 15-12	5555
U 15-13	P5AC
U 15-14	5555
U 15-15	2AAA
U 17- 1	high
U 17- 2	8AF9
U 17- 3	PA66
U 17- 4	6AA7
U 17- 5	low
U 17- 6	low
U 17- 7	P5AC
U 17- 9	low
U 17-10	low
U 17-11	5555
U 17-12	4764
U 17-13	2AAA
U 17-14	1HP7
U 17-15	low
U 34- 1	high
U 34- 2	CP17
U 34- 3	HPC8

```
U 34- 4  CP17
U 34- 6  F35U
U 34- 7  A3U0
U 34- 9  F35U
U 34-13  4996
U 34-14  2939
U 34-15  high
U 35- 1  high
U 35- 2  HPC8
U 35- 3  CP17
U 35- 4  2939
U 35- 5  U781
U 35- 6  972P
U 35- 7  4996
U 35- 9  low
U 35-10  2939
U 35-11  8AF9
U 35-12  PA66
U 35-13  4996
U 35-14  F35U
U 35-15  A3U0
U 49- 7  894F
U 49-11  low
U 49-15  HF59
U 54- 1  high
U 54- 2  C1FU
U 54- 3  C1FU
U 54- 4  U498
U 54- 5  A76H
U 54- 6  24FP
U 54- 7  UUPC
U 54- 9  8622
U 54-10  6476
U 54-11  F29U
U 54-12  C1FU
U 54-13  low
U 54-14  C1FU
U 54-15  H160
U 55- 1  high
U 55- 2  HF59
U 55- 3  CC05
U 55- 4  UC7H
U 55- 5  A3CU
U 55- 6  low
U 55- 7  low
U 55- 9  H160
U 55-10  low
U 55-11  C5F8
U 55-12  894F
U 55-13  U6UA
U 55-14  CU90
U 55-15  low
U 64- 7  P0H1
U 64-11  PU50
U 64-15  low
U 71- 1  high
U 71- 2  C1C7
U 71- 3  8823
U 71- 4  94P9
U 71- 5  F29U
U 71- 6  C1C7
U 71- 7  8823
U 71- 9  0000
(TOTLZ=0130)
U 71-10  94P9
U 71-11  PHU4
U 71-12  U6UA
U 71-13  PHU4
U 71-14  U6UA
U 71-15  UC7H
U 73- 1  high
U 73- 2  AA7A
U 73- 3  A245
U 73- 4  01HA
U 73- 5  H0C7
U 73- 6  AA7A
U 73- 7  A245
U 73- 9  0000
(TOTLZ=0130)
U 73-10  01HA
U 73-11  A76H
U 73-12  24FP
U 73-13  A76H
U 73-14  24FP
U 73-15  F29U
```

64601A Timing Control Board
OR #14

NORM MODE VH = 60AU

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 pos. edge
Location of GROUND: gnd

TTL

U 49- 4	179F
U 49- 5	P6PC
U 49-12	low
U 49-13	6F62
U 64- 4	low
U 64- 5	A056
U 64-12	3UU6
U 64-13	low
U 85- 1	60AU
(TOTLZ=0004)	
U 85- 2	179F
U 85- 3	H4CU
U 85- 4	P6PC
U 85- 5	6H5P
U 85- 6	low
U 85- 7	6HF7
U 85- 8	low
U 85- 9	55P2
U 85-11	3UU6
U 85-12	2H1C
U 85-13	A056
U 85-14	HU32
U 85-15	6390
U 85-16	1278
U 85-17	low
U 85-18	05C6
U 85-19	60AU
(TOTLZ=0004)	

ECL

U 10- 1	high
U 10- 2	3542
U 10- 3	CH21
U 10- 4	5P90
U 10- 5	8474
U 10- 6	3542
U 10- 7	CH21
U 10- 9	0000
(TOTLZ=0130)	
U 10-10	5P90
U 10-11	H830
U 10-12	FC98
U 10-13	H830
U 10-14	FC98
U 10-15	65FF
U 11- 1	high
U 11- 2	0934
U 11- 3	049A
U 11- 4	U535
U 11- 5	1268
U 11- 6	0934
U 11- 7	049A
U 11- 9	0000
(TOTLZ=0130)	
U 11-10	U535
U 11-11	2A62
U 11-12	C2C1
U 11-13	2A62
U 11-14	C2C1
U 11-15	5958
U 13- 1	high
U 13- 2	2607
U 13- 3	46A8
U 13- 4	U535
U 13- 5	low
U 13- 6	low
U 13- 7	2A62
U 13- 9	low
U 13-10	low
U 13-11	C2C1
U 13-12	2F99
U 13-13	5958
U 13-14	7551
U 13-15	low
U 15- 1	high
U 15- 2	AFAF
U 15- 3	H656
U 15- 4	1F53
U 15- 5	5958
U 15- 6	AFAF
U 15- 7	H656
U 15- 9	0000
(TOTLZ=0130)	
U 15-10	1F53
U 15-11	5PH1
U 15-12	08P8
U 15-13	5PH1
U 15-14	08P8
U 15-15	8474
U 17- 1	high
U 17- 2	614H
U 17- 3	01P2
U 17- 4	1F53
U 17- 5	low
U 17- 6	low
U 17- 7	5PH1
U 17- 9	low
U 17-10	low
U 17-11	08P8
U 17-12	2F99
U 17-13	8474
U 17-14	7551
U 17-15	low
U 34- 1	high
U 34- 2	PH9U
U 34- 3	8H30

```
U 34- 4  PH9U
U 34- 6  AAH5
U 34- 7  FA7A
U 34- 9  AAH5
U 34-13  FC98
U 34-14  AC37
U 35- 1  high
U 35- 2  8H30
U 35- 3  PH9U
U 35- 4  AC37
U 35- 5  2607
U 35- 6  46A8
U 35- 7  FC98
U 35- 9  low
U 35-10  AC37
U 35-11  614H
U 35-12  01P2
U 35-13  FC98
U 35-14  AAH5
U 35-15  FA7A
U 49- 7  P6PC
U 49-11  low
U 49-15  6F62
U 54- 1  high
U 54- 2  C1FU
U 54- 3  C1FU
U 54- 4  07HC
U 54- 5  C2C4
U 54- 6  AP22
U 54- 7  5CCF
U 54- 9  8622
U 54-10  46FH
U 54-11  87P9
U 54-12  C1FU
U 54-13  low
U 54-14  C1FU
U 54-15  H160
U 55- 1  high
U 55- 2  6F62
U 55- 4  1268
U 55- 5  8C70
U 55- 6  low
U 55- 7  low
U 55- 9  H160
U 55-10  low
U 55-11  5938
U 55-12  P6PC
U 55-13  24H1
U 55-14  0HF8
U 55-15  low
U 64- 7  A056
U 64-11  3UU6
U 64-15  low
U 71- 1  high
U 71- 2  930F
U 71- 3  197P
U 71- 4  HF47
U 71- 5  87P9
U 71- 6  930F
U 71- 7  197P
U 71- 9  0000
(TOTLZ=0130)
U 71-10  HF47
U 71-11  49A3
U 71-12  24H1
U 71-13  49A3
U 71-14  24H1
U 71-15  1268
U 73- 1  high
U 73- 2  04C2
U 73- 3  U521
U 73- 4  2A68
U 73- 5  8H26
U 73- 6  04C2
U 73- 7  U521
U 73- 9  0000
(TOTLZ=0130)
U 73-10  2A68
U 73-11  C2C4
U 73-12  AP22
U 73-13  C2C4
U 73-14  AP22
U 73-15  87P9
```

64601A Timing Control Board
B FOLLOWED BY A # 15

NORM MODE VH = F15U

DATA THRESHOLD HIGH: ttl & ecl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: tp 12 neg. edge
Location of QUAL/STOP: tp 12 pos. edge
Location of CLOCK: tp 11 pos. edge
Location of GROUND: gnd

TTL

U 49- 4	AC98
U 49- 5	1888
U 49-12	low
U 49-13	1888
U 64- 4	low
U 64- 5	743F
U 64-12	CHF6
U 64-13	low
U 85- 1	F15U
(TOTLZ=0005)	
U 85- 2	AC98
U 85- 3	23H2
U 85- 4	1888
U 85- 5	F413
U 85- 6	low
U 85- 7	48P7
U 85- 8	low
U 85- 9	7150
U 85-11	CHF6
U 85-12	CC9C
U 85-13	743F
U 85-14	1453
U 85-15	F721
U 85-16	67C5
U 85-17	low
U 85-18	338A
U 85-19	F15U
(TOTLZ=0005)	

ECL

U 10- 1	high
U 10- 2	13H7
U 10- 3	F6PA
U 10- 4	6375
U 10- 5	644P
U 10- 6	13H7
U 10- 7	F6PA
U 10- 9	0000
(TOTLZ=0130)	
U 10-10	6375
U 10-11	HU4C
U 10-12	FP55
U 10-13	HU4C
U 10-14	FP55
U 10-15	A82C
U 11- 1	high
U 11- 2	A451
U 11- 3	H228
U 11- 4	87P5
U 11- 5	48A2
U 11- 6	A451
U 11- 7	H228
U 11- 9	0000
(TOTLZ=0130)	
U 11-10	87P5
U 11-11	P202
U 11-12	H0U1
U 11-13	P202
U 11-14	H0U1
U 11-15	2779
U 13- 1	high
U 13- 2	P118
U 13- 3	2047
U 13- 4	87P5
U 13- 5	low
U 13- 6	low
U 13- 7	P202
U 13- 9	low
U 13-10	low
U 13-11	H0U1
U 13-13	2779
U 13-14	35H5
U 13-15	low
U 15- 1	high
U 15- 2	13CF
U 15- 3	89HP
U 15- 4	2A1P
U 15- 5	2779
U 15- 6	13CF
U 15- 7	89HP
U 15- 9	0000
(TOTLZ=0130)	
U 15-10	2A1P
U 15-11	C4UU
U 15-12	157P
U 15-13	C4UU
U 15-14	157P
U 15-15	644P
U 17- 1	high
U 17- 2	A5PC
U 17- 3	64C4
U 17- 4	2A1P
U 17- 5	low
U 17- 6	low
U 17- 7	C4UU
U 17- 9	low
U 17-10	low
U 17-11	157P
U 17-13	644P
U 17-14	35H5
U 17-15	low
U 42- 1	high
U 42- 3	C7P0
U 42- 4	high
U 42- 5	F1PA
U 42- 6	A451

```
U 42- 7  2U4H
U 42- 9  low
U 42-10  high
U 42-11  73FH
U 42-12  13CF
U 42-13  6CCP
U 42-14  F102
U 42-15  005H
U 54- 1  high
U 54- 2  C036
U 54- 3  C036
U 54- 4  4H2A
U 54- 5  6U6F
U 54- 6  5947
U 54- 7  9P91
U 54- 9  8P42
U 54-10  F82C
U 54-11  0H53
U 54-12  C036
U 54-13  low
U 54-14  C036
U 54-15  7169
U 55- 1  high
U 55- 2  1888
U 55- 4  48A2
U 55- 5  C7P0
U 55- 6  low
U 55- 7  low
U 55- 9  7169
U 55-10  low
U 55-11  509P
U 55-12  80CP
U 55-13  0U46
U 55-14  F102
U 55-15  low
U 64- 7  743F
U 64-11  CHF6
U 64-15  low
U 67- 1  high
U 67- 2  H882
U 67- 3  low
U 67- 4  005H
U 67- 5  8P42
U 67- 6  725F
U 67- 7  H9H7
U 67- 9  8P42
U 67-10  1888
U 67-11  A759
U 67-12  8P42
U 67-13  low
U 67-14  6606
U 67-15  high
U 69- 1  high
U 69- 2  low
U 69- 3  0000
(TOTLZ=0130)
U 69- 4  5949
U 69- 5  low
U 69- 6  0000
(TOTLZ=0170)
U 69- 7  8P42
U 69- 9  3240
U 69-10  8P42
U 69-11  8P42
U 69-12  U31U
U 69-13  high
U 69-14  U31U
U 71- 1  high
U 71- 2  A759
U 71- 3  725F
U 71- 4  18HP
U 71- 5  0H53
U 71- 6  A759
U 71- 7  725F
U 71- 9  0000
(TOTLZ=0130)
U 71-10  18HP
U 71-11  F36P
U 71-12  0U46
U 71-13  F36P
U 71-14  0U46
U 71-15  48A2
U 73- 1  high
U 73- 2  5949
U 73- 3  F255
U 73- 4  40HA
U 73- 5  546U
U 73- 6  5949
U 73- 7  F255
U 73- 9  0000
(TOTLZ=0130)
U 73-10  40HA
U 73-11  6U6F
U 73-12  5947
U 73-13  6U6F
U 73-14  5947
U 73-15  0H53
U 74- 1  high
U 74- 2  80CP
U 74- 4  8P42
U 74- 5  H882
U 74-10  5949
U 74-11  6606
U 74-12  low
U 74-13  8P42
U 74-14  high
```

64601A Timing Control Board
DISPLAY TEST- 1ST PATTERN

QUAL MODE VH = 383A

Qual = high

DATA THRESHOLD: ttl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: tp 10 pos. edge
Location of QUAL/STOP: U99-12 or U 81-13 pos. edge
Location of CLOCK: tp 8 pos. edge
Location of GROUND: gnd

TTL

U 56- 1	high	U 58-16	5AFC	U 59-16	5AFC	U 61- 4	high
U 56- 2	low	U 58-17	5632	U 59-17	5632	U 61- 5	383A
U 56- 5	high	U 59- 1	P816	U 60- 1	low	(TOTLZ=0025)	
U 56- 7	high	U 59- 2	580H	U 60- 2	P816	U 61- 6	0000
U 56- 9	high	U 59- 3	12A9	U 60- 3	H02F	(TOTLZ=0024)	
U 56-10	high	U 59- 4	UPF6	U 60- 4	6037	U 61- 9	383A
U 56-12	low	U 59- 5	8779	U 60- 5	C01C	(TOTLZ=0001)	
U 56-15	high	U 59- 6	82PU	U 60- 6	9549	U 61-10	high
U 57- 1	P816	U 59- 7	2A93	U 60- 7	2A93	U 61-11	CC34
U 57- 2	580H	U 59- 8	high	U 60- 8	9549	U 61-12	CC34
U 57- 3	12A9	U 59-10	low	U 60- 9	4AA4	U 61-13	383A
U 57- 4	UPF6	U 59-12	4CP2	U 60-11	0000	(TOTLZ=0024)	
U 57- 5	8779	U 59-13	HU2A	(TOTLZ=12519)		U 61-14	383A
U 57- 6	82PU	U 59-14	4521	U 60-12	H02F	U 61-15	383A
U 57- 7	H02F	U 59-15	986C	U 60-13	P816	(TOTLZ=0024)	
U 57- 8	high	U 59-16	5AFC	U 60-14	C01C	U 62- 1	high
U 57-10	low	U 59-17	5632	U 60-15	580H	U 62- 2	high
U 57-12	4CP2	U 60- 1	low	U 60-16	637P	U 62- 3	0000
U 57-13	HU2A	U 60- 2	P816	U 60-17	F6UF	(TOTLZ=12519)	
U 57-14	4521	U 60- 3	H02F	U 60-19	high	U 62- 4	0000
U 57-15	986C	U 60- 4	6037	U 61- 1	383A	(TOTLZ=12519)	
U 57-16	5AFC	U 60- 5	C01C	U 61- 2	1166	U 62- 5	0000
U 57-17	5632	U 60- 6	9549	U 61- 3	1166	(TOTLZ=12519)	
U 58- 1	P816	U 60- 7	2A93			U 62- 6	383A
U 58- 2	580H	U 60- 8	9549			(TOTLZ=0024)	
U 58- 3	12A9	U 60- 9	4AA4			U 62- 7	383A
U 58- 4	UPF6	U 60-11	0000			(TOTLZ=0024)	
U 58- 5	8779	(TOTLZ=12519)				U 62- 9	U352
U 58- 6	82PU	U 60-12	H02F			U 62-10	U352
U 58- 7	6037	U 60-13	P816			U 62-11	1166
U 58- 8	high	U 60-14	C01C			U 62-12	383A
U 58-10	low	U 60-15	580H			(TOTLZ=0001)	
U 58-12	4CP2	U 60-16	637P			U 62-13	383A
U 58-13	HU2A	U 60-17	F6UF			U 62-14	high
U 58-14	4521	U 60-19	high			U 62-15	low
U 58-15	986C	U 61- 1	383A			U 63- 1	high
		U 61- 2	1166			U 63- 2	383A
		U 61- 3	1166			(TOTLZ=0024)	

```
U 63- 4  high
U 63- 5  383A
(TOTLZ=0024)
U 63- 6  0000
(TOTLZ=0024)
U 63- 8  383A
(TOTLZ=12518)
U 63- 9  0000
(TOTLZ=12519)
U 63-10  high
U 63-12  383A
(TOTLZ=12518)
U 63-13  high
U 76- 1  high
U 76- 2  H02F
U 76- 4  6037
U 76- 6  2A93
U 76-10  F6UF
U 76-12  CAH5
U 76-14  CU43
U 76-15  high
U 77- 1  UPF6
U 77- 2  12A9
U 77- 3  580H
U 77- 4  P816
U 77- 5  82PU
U 77- 6  5632
U 77- 7  5AFC
U 77- 8  low
U 77-10  CU43
U 77-12  F6UF
U 77-13  high
U 77-14  high
U 77-16  CAH5
U 77-17  high
U 77-18  low
U 77-19  low
U 77-20  high
U 77-21  8779
U 77-22  high
U 78- 1  high
U 78- 2  383A
(TOTLZ=0024)
U 78- 3  high
U 78- 4  low
U 78- 5  low
U 78- 6  low
U 78- 7  high
U 78- 9  FC68
U 78-10  high
U 78-11  AHAU
U 78-12  9023
U 78-13  CU1A
U 78-14  AU73
U 78-15  U352
U 79- 1  low
U 79- 2  high
U 79- 3  986C
U 79- 4  AHAU
U 79- 5  AU73
U 79- 6  CU1A
U 79- 7  9023
U 79- 9  0U22
U 79-10  9286
U 79-11  7923
U 79-12  PH28
U 79-13  low
U 79-14  low
U 79-15  low
U 80- 1  580H
U 80- 2  C01C
U 80- 3  H02F
U 80- 4  P816
U 80- 5  PH28
U 80- 6  7923
U 80- 7  9286
U 80- 9  CH6F
U 80-10  8556
U 80-11  A900
U 80-12  842U
U 80-13  low
U 80-14  low
U 80-15  low
U 81- 1  high
U 81- 2  HUA1
U 81- 3  CU43
U 81- 4  HUA1
U 81- 5  6UH0
U 81- 6  CAH5
U 81- 7  5H6A
U 81- 9  0000
(TOTLZ=12519)
U 81-10  APC5
U 81-11  5H6A
U 81-12  14AP
U 81-13  383A
(TOTLZ=0001)
U 81-14  883F
U 81-15  C383
U 82- 1  low
U 82- 2  low
U 82- 3  high
U 82- 4  low
U 82- 5  low
U 82- 6  high
U 82- 8  high
U 82- 9  low
U 82-10  high
U 82-11  low
U 82-12  high
U 82-13  high
U 83- 1  637P
U 83- 2  A1FH
U 83- 3  383A
(TOTLZ=12518)
U 83- 4  0000
(TOTLZ=12519)
U 83- 5  993F
U 83- 6  99U7
U 83- 8  883F
U 83- 9  8556
U 83-10  14AP
U 83-13  14AP
U 84- 1  high
U 84- 2  0000
U 84- 3  383A
(TOTLZ=0024)
U 84- 4  high
U 84- 5  0000
U 84- 6  383A
U 84- 8  low
U 84- 9  high
U 84-10  high
U 84-11  0000
U 84-12  high
U 84-13  high
U 88- 1  low
U 88- 2  high
U 88- 4  low
U 88- 8  C383
U 88- 9  99U7
U 88-10  FF2A
U 88-11  low
U 88-12  U352
U 88-13  FC68
U 89- 1  low
U 89- 2  low
U 89- 4  low
U 89- 5  low
U 89- 8  low
U 89-11  low
U 90- 4  low
U 90- 5  high
U 90- 6  high
U 90- 7  low
U 90- 9  low
U 90-10  low
U 90-11  low
U 90-12  high
U 90-14  high
U 90-15  high
U 91- 6  high
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U 91- 7  high
U 91- 9  high
U 91-10  high
U 91-11  high
U 91-12  high
U 91-13  high
U 91-14  high
U 91-15  high
U 92- 1  high
U 92- 2  high
U 92- 5  low
U 92- 7  low
U 92- 9  high
U 92-10  low
U 92-12  high
U 92-15  high
U 93- 1  high
U 93- 2  low
U 93- 5  low
U 93- 7  low
U 93- 9  high
U 93-10  high
U 93-12  high
U 93-15  high
U 94- 1  high
U 94- 2  0000
(TOTLZ=12519)
U 94- 3  high
U 94- 4  low
U 94- 5  low
U 94- 6  low
U 94- 7  high
U 94- 9  383A
(TOTLZ=0024)
U 94-10  high
U 94-11  UPF6
U 94-12  12A9
U 94-13  580H
U 94-14  P816
U 94-15  898A
U 95- 1  high
U 95- 2  0000
(TOTLZ=12519)
U 95- 3  high
U 95- 4  high
U 95- 5  low
U 95- 6  low
U 95- 7  high
U 95- 9  383A
(TOTLZ=0024)
U 95-10  898A
U 95-11  5AFC
U 95-12  5632
U 95-13  82PU
U 95-14  8779
U 95-15  1166
U 96- 1  high
U 96- 2  383A
(TOTLZ=0024)
U 96- 3  low
U 96- 4  high
U 96- 5  high
U 96- 6  high
U 96- 7  high
U 96- 9  383A
(TOTLZ=0001)
U 96-10  U352
U 96-11  4CP2
U 96-12  HU2A
U 96-13  4521
U 96-14  986C
U 96-15  CC34
U 97- 1  4743
U 97- 2  87AA
U 97- 3  8C0U
U 97- 4  4AA4
U 97- 5  4743
U 97- 6  FA9P
U 97- 8  FA9P
U 97- 9  0U22
U 97-10  0000
U 97-11  968U
U 97-12  APC5
U 97-13  383A
(TOTLZ=12518)
U 98- 1  high
U 98- 2  4743
U 98- 3  7U79
U 98- 4  FF2A
U 98- 5  4AA4
U 98- 6  729P
U 98- 7  4AA4
U 98- 9  383A
(TOTLZ=25037)
U 98-10  87AA
U 98-11  CU90
U 98-12  87AA
U 98-13  968U
U 98-14  0000
U 98-15  383A
U 99- 1  383A
(TOTLZ=0001)
U 99- 2  383A
(TOTLZ=0025)
U 99- 3  14AP
U 99- 4  5H6A
U 99- 5  5H6A
U 99- 6  5H6A
U 99- 8  87AA
U 99- 9  6UH0
U 99-10  6UH0
U 99-11  4AA4
U 99-12  383A
(TOTLZ=0001)
U 99-13  high
U100- 1  high
U100- 2  842U
U100- 3  0000
(TOTLZ=12519)
U100- 4  high
U100- 5  A1FH
U100- 6  99U7
U100- 8  A106
U100- 9  993F
U100-10  high
U100-11  0000
(TOTLZ=12519)
U100-12  A900
U100-13  high
U101- 1  383A
U101- 2  0000
U101- 4  low
U101- 5  0000
(TOTLZ=25038)
U101-10  low
U101-11  high
U101-12  high
U101-13  low
```

64601A Timing Control Board
DISPLAY TEST- 2ND PATTERN

QUAL MODE VH = 383A

Qual = high

DATA THRESHOLD: ttl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: tp 10 pos. edge
Location of QUAL/STOP: U99-12 or U 81-13 pos. edge
Location of CLOCK: tp 8 pos. edge
Location of GROUND: gnd

TTL

U 56- 1	high	U 58-16	5AFC	U 61- 4	high
U 56- 2	low	U 58-17	5632	U 61- 5	383A
U 56- 5	low	U 59- 1	P816	(TOTLZ=0025)	
U 56- 7	high	U 59- 2	580H	U 61- 6	0000
U 56- 9	high	U 59- 3	12A9	(TOTLZ=0024)	
U 56-10	high	U 59- 4	UPF6	U 61- 7	0000
U 56-12	low	U 59- 5	8779	U 61- 9	383A
U 56-15	high	U 59- 6	82PU	(TOTLZ=0001)	
U 57- 1	P816	U 59- 7	2A93	U 61-10	high
U 57- 2	580H	U 59- 8	high	U 61-11	CC34
U 57- 3	12A9	U 59-10	low	U 61-12	CC34
U 57- 4	UPF6	U 59-12	4CP2	U 61-13	383A
U 57- 5	8779	U 59-13	HU2A	(TOTLZ=0024)	
U 57- 6	82PU	U 59-14	4521	U 61-14	383A
U 57- 7	H02F	U 59-15	986C	U 61-15	383A
U 57- 8	high	U 59-16	5AFC	(TOTLZ=0024)	
U 57-10	low	U 59-17	5632	U 62- 1	high
U 57-12	4CP2	U 60- 1	low	U 62- 2	high
U 57-13	HU2A	U 60- 2	P816	U 62- 3	0000
U 57-14	4521	U 60- 3	H02F	(TOTLZ=12519)	
U 57-15	986C	U 60- 4	6037	U 62- 4	0000
U 57-16	5AFC	U 60- 5	C01C	(TOTLZ=12519)	
U 57-17	5632	U 60- 6	9549	U 62- 5	0000
U 58- 1	P816	U 60- 7	2A93	(TOTLZ=12519)	
U 58- 2	580H	U 60- 8	9549	U 62- 6	383A
U 58- 3	12A9	U 60- 9	4AA4	(TOTLZ=0024)	
U 58- 4	UPF6	U 60-11	0000	U 62- 7	383A
U 58- 5	8779	(TOTLZ=12519)		(TOTLZ=0024)	
U 58- 6	82PU	U 60-12	H02F	U 62- 9	U352
U 58- 7	6037	U 60-13	P816	U 62-10	U352
U 58- 8	high	U 60-14	C01C	U 62-11	1166
U 58-10	low	U 60-15	580H	U 62-12	383A
U 58-12	4CP2	U 60-16	637P	(TOTLZ=0001)	
U 58-13	HU2A	U 60-17	F6UF	U 62-13	383A
U 58-14	4521	U 61- 1	383A	U 62-14	high
U 58-15	986C	(TOTLZ=12518)		U 62-15	low
		U 61- 2	1166	U 63- 1	high
		U 61- 3	1166		

U 63- 2 383A
(TOTLZ=0024)
U 63- 4 high
U 63- 5 383A
(TOTLZ=0024)
U 63- 6 0000
(TOTLZ=0024)
U 63- 8 383A
(TOTLZ=12518)
U 63- 9 0000
(TOTLZ=12519)
U 63-10 high
U 63-12 383A
(TOTLZ=12518)
U 63-13 high
U 76- 1 high
U 76- 2 H02F
U 76- 4 6037
U 76- 6 2A93
U 76-10 F6UF
U 76-12 CAH5
U 76-14 CU43
U 76-15 high
U 77- 1 UPF6
U 77- 2 12A9
U 77- 3 580H
U 77- 4 P816
U 77- 5 82PU
U 77- 6 5632
U 77- 7 5AFC
U 77- 8 low
U 77-10 CU43
U 77-12 F6UF
U 77-13 high
U 77-14 high
U 77-16 CAH5
U 77-17 high
U 77-18 low
U 77-19 low
U 77-20 high
U 77-21 8779
U 77-22 high
U 78- 1 high
U 78- 2 383A
(TOTLZ=0024)
U 78- 3 high
U 78- 4 low
U 78- 5 low
U 78- 6 low
U 78- 7 high
U 78- 9 FC68
U 78-10 high
U 78-11 AHAU
U 78-12 9023
U 78-13 CU1A
U 78-14 AU73
U 78-15 U352
U 79- 1 low
U 79- 2 low
U 79- 3 986C
U 79- 4 AHAU
U 79- 5 AU73
U 79- 6 CU1A
U 79- 7 9023
U 79- 9 0U22
U 79-10 C584
U 79-11 FF3U
U 79-12 2033
U 79-13 low
U 79-14 low
U 79-15 low
U 80- 1 580H
U 80- 2 C01C
U 80- 3 H02F
U 80- 4 P816
U 80- 5 2033
U 80- 6 FF3U
U 80- 7 C584
U 80- 9 8054
U 80-10 C86P
U 80-11 H49C
U 80-12 368C
U 80-13 low
U 80-14 low
U 80-15 low
U 81- 1 high
U 81- 2 HUA1
U 81- 3 CU43
U 81- 4 HUA1
U 81- 5 6UH0
U 81- 6 CAH5
U 81- 7 5H6A
U 81- 9 0000
(TOTLZ=12519)
U 81-10 APC5
U 81-11 5H6A
U 81-12 14AP
U 81-13 383A
(TOTLZ=0001)
U 81-14 1281
U 81-15 H04A
U 82- 1 low
U 82- 2 low
U 82- 3 high
U 82- 4 low
U 82- 5 low
U 82- 6 high
U 82- 8 high
U 82- 9 low
U 82-10 high
U 82-11 low
U 82-12 high
U 82-13 high
U 83- 1 637P
U 83- 2 HC3C
U 83- 3 383A
(TOTLZ=12518)
U 83- 4 0000
U 83- 5 4C46
U 83- 6 P301
U 83- 8 1281
U 83- 9 C86P
U 83-10 14AP
U 83-13 14AP
U 84- 1 high
U 84- 2 0000
U 84- 3 383A
(TOTLZ=0024)
U 84- 4 high
U 84- 5 0000
U 84- 6 383A
U 84- 8 low
U 84- 9 high
U 84-10 high
U 84-11 0000
U 84-12 high
U 84-13 high
U 88- 1 low
U 88- 2 high
U 88- 4 low
U 88- 8 H04A
U 88- 9 P301
U 88-10 9PCU
U 88-11 low
U 88-12 U352
U 88-13 FC68
U 89- 1 low
U 89- 2 low
U 89- 4 low
U 89- 5 low
U 89- 8 low
U 89-11 low
U 90- 4 low
U 90- 5 high
U 90- 6 high
U 90- 7 low
U 90- 9 low
U 90-10 low
U 90-11 low
U 90-12 high
U 90-14 high
U 90-15 high

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U 91- 6  high
U 91- 7  high
U 91- 9  high
U 91-10  high
U 91-11  high
U 91-12  high
U 91-13  high
U 91-14  high
U 91-15  high
U 92- 1  high
U 92- 2  high
U 92- 5  low
U 92- 7  low
U 92- 9  high
U 92-10  low
U 92-12  high
U 92-15  high
U 93- 1  high
U 93- 2  low
U 93- 5  low
U 93- 7  low
U 93- 9  high
U 93-10  high
U 93-12  high
U 93-15  high
U 94- 1  high
U 94- 2  0000
(TOTLZ=12519)
U 94- 3  high
U 94- 4  low
U 94- 5  low
U 94- 6  low
U 94- 7  high
U 94- 9  383A
(TOTLZ=0024)
U 94-10  high
U 94-11  UPF6
U 94-12  12A9
U 94-13  580H
U 94-14  P816
U 94-15  898A
U 95- 1  high
U 95- 2  0000
(TOTLZ=12519)
U 95- 3  high
U 95- 4  high
U 95- 5  low
U 95- 6  low
U 95- 7  high
U 95- 9  383A
(TOTLZ=0024)
U 95-10  898A
U 95-11  5AFC
U 95-12  5632
U 95-13  82PU
U 95-14  8779
U 95-15  1166
U 96- 1  high
U 96- 2  383A
(TOTLZ=0024)
U 96- 3  low
U 96- 4  high
U 96- 5  high
U 96- 6  high
U 96- 7  high
U 96- 9  383A
(TOTLZ=0001)
U 96-10  U352
U 96-11  4CP2
U 96-12  HU2A
U 96-13  4521
U 96-14  986C
U 96-15  CC34
U 97- 1  U4UC
U 97- 2  87AA
U 97- 3  A8H9
U 97- 4  4AA4
U 97- 5  U4UC
U 97- 6  15PA
U 97- 8  15PA
U 97- 9  0U22
U 97-10  0000
U 97-11  968U
U 97-12  APC5
U 97-13  383A
(TOTLZ=12518)
U 98- 1  high
U 98- 2  U4UC
U 98- 3  FFF1
U 98- 4  9PCU
U 98- 5  4AA4
U 98- 6  729P
U 98- 7  4AA4
U 98- 9  383A
(TOTLZ=25037)
U 98-10  87AA
U 98-11  CU90
U 98-12  87AA
U 98-13  968U
U 98-14  0000
U 98-15  383A
U 99- 1  383A
(TOTLZ=0001)
U 99- 2  383A
(TOTLZ=0025)
U 99- 3  14AP
U 99- 4  5H6A
U 99- 5  5H6A
U 99- 6  5H6A
U 99- 8  87AA
U 99- 9  6UH0
U 99-10  6UH0
U 99-11  4AA4
U 99-12  383A
(TOTLZ=0001)
U 99-13  high
U100- 1  high
U100- 2  368C
U100- 3  0000
(TOTLZ=12519)
U100- 4  high
U100- 5  HC3C
U100- 6  P301
U100- 8  737F
U100- 9  4C46
U100-10  high
U100-11  0000
U100-12  H49C
U100-13  high
U101- 1  383A
U101- 2  0000
U101- 4  low
U101- 5  0000
(TOTLZ=25038)
U101-10  low
U101-11  high
U101-12  high
U101-13  low
```

64601A Timing Control Board
DISPLAY TEST- 3RD PATTERN

QUAL MODE VH = 383A

Qual = high

DATA THRESHOLD: ttl
CLOCK THRESHOLD: ttl
ST-SP-QL THRESHOLD: ttl

Location of ST/SP/START: tp 10 pos. edge
Location of QUAL/STOP: U99-12 or U81-13 pos. edge
Location of CLOCK: tp 8 pos. edge
Location of GROUND: gnd

TTL

U 56- 1	high	U 58-16	5AFC	U 61- 4	high
U 56- 2	high	U 58-17	5632	U 61- 5	383A
U 56- 5	high	U 59- 1	P816	(TOTLZ=0025)	
U 56- 7	high	U 59- 2	580H	U 61- 6	0000
U 56- 9	high	U 59- 3	12A9	(TOTLZ=0024)	
U 56-10	high	U 59- 4	UPF6	U 61- 7	0000
U 56-12	low	U 59- 5	8779	U 61- 9	383A
U 56-15	high	U 59- 6	82PU	(TOTLZ=0001)	
U 57- 1	P816	U 59- 7	2A93	U 61-10	high
U 57- 2	580H	U 59- 8	high	U 61-11	CC34
U 57- 3	12A9	U 59-10	low	U 61-12	CC34
U 57- 4	UPF6	U 59-12	4CP2	U 61-13	383A
U 57- 5	8779	U 59-13	HU2A	(TOTLZ=0024)	
U 57- 6	82PU	U 59-14	4521	U 61-14	383A
U 57- 7	H02F	U 59-15	986C	U 61-15	383A
U 57- 8	high	U 59-16	5AFC	(TOTLZ=0024)	
U 57-10	low	U 59-17	5632	U 62- 1	high
U 57-12	4CP2	U 60- 1	low	U 62- 2	high
U 57-13	HU2A	U 60- 2	P816	U 62- 3	0000
U 57-14	4521	U 60- 3	H02F	(TOTLZ=12519)	
U 57-15	986C	U 60- 4	6037	U 62- 4	0000
U 57-16	5AFC	U 60- 5	C01C	(TOTLZ=12519)	
U 57-17	5632	U 60- 6	9549	U 62- 5	0000
U 58- 1	P816	U 60- 7	2A93	(TOTLZ=12519)	
U 58- 2	580H	U 60- 8	9549	U 62- 6	383A
U 58- 3	12A9	U 60- 9	4AA4	(TOTLZ=0024)	
U 58- 4	UPF6	U 60-11	0000	U 62- 7	383A
U 58- 5	8779	(TOTLZ=12519)		(TOTLZ=0024)	
U 58- 6	82PU	U 60-12	H02F	U 62- 9	U352
U 58- 7	6037	U 60-13	P816	U 62-10	U352
U 58- 8	high	U 60-14	C01C	U 62-11	1166
U 58-10	low	U 60-15	580H	U 62-12	383A
U 58-12	4CP2	U 60-16	637P	(TOTLZ=0001)	
U 58-13	HU2A	U 60-17	F6UF	U 62-13	383A
U 58-14	4521	U 61- 1	383A	U 62-14	high
U 58-15	986C	(TOTLZ=12518)		U 62-15	low
		U 61- 2	1166	U 63- 1	high
		U 61- 3	1166		

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U 63- 2  383A
(TOTLZ=0024)
U 63- 4  high
U 63- 5  383A
(TOTLZ=0024)
U 63- 6  0000
(TOTLZ=0024)
U 63- 8  383A
(TOTLZ=12518)
U 63- 9  0000
(TOTLZ=12519)
U 63-10  high
U 63-12  383A
(TOTLZ=12518)
U 63-13  high
U 76- 1  high
U 76- 2  H02F
U 76- 4  6037
U 76- 6  2A93
U 76-10  F6UF
U 76-12  CAH5
U 76-14  CU43
U 76-15  high
U 77- 1  UPF6
U 77- 2  12A9
U 77- 3  580H
U 77- 4  P816
U 77- 5  82PU
U 77- 6  5632
U 77- 7  5AFC
U 77- 8  low
U 77-10  CU43
U 77-12  F6UF
U 77-13  high
U 77-14  high
U 77-16  CAH5
U 77-17  high
U 77-18  low
U 77-19  low
U 77-20  high
U 77-21  8779
U 77-22  high
U 78- 1  high
U 78- 2  383A
(TOTLZ=0024)
U 78- 3  high
U 78- 4  low
U 78- 5  low
U 78- 6  low
U 78- 7  high
U 78- 9  FC68
U 78-10  high
U 78-11  AHAU
U 78-12  9023
U 78-13  CU1A
U 78-14  AU73
U 78-15  U352
U 79- 1  low
U 79- 2  high
U 79- 3  986C
U 79- 4  AHAU
U 79- 5  AU73
U 79- 6  CU1A
U 79- 7  9023
U 79- 9  0U22
U 79-10  9286
U 79-11  7923
U 79-12  PH28
U 79-13  low
U 79-14  low
U 79-15  low
U 80- 1  580H
U 80- 2  C01C
U 80- 3  H02F
U 80- 4  P816
U 80- 5  PH28
U 80- 6  7923
U 80- 7  9286
U 80- 9  CH6F
U 80-10  8556
U 80-11  1716
U 80-12  A424
U 80-13  low
U 80-14  low
U 80-15  high
U 81- 1  high
U 81- 2  HUA1
U 81- 3  CU43
U 81- 4  HUA1
U 81- 5  6UH0
U 81- 6  CAH5
U 81- 7  5H6A
U 81- 9  0000
(TOTLZ=12519)
U 81-10  APC5
U 81-11  5H6A
U 81-12  14AP
U 81-13  383A
(TOTLZ=0001)
U 81-14  883F
U 81-15  C383
U 82- 1  low
U 82- 2  low
U 82- 3  high
U 82- 4  low
U 82- 5  low
U 82- 6  high
U 82- 8  high
U 82- 9  low
U 82-10  high
U 82-11  low
U 82-12  high
U 82-13  high
U 83- 1  637P
U 83- 2  31F8
U 83- 3  383A
(TOTLZ=12518)
U 83- 4  0000
(TOTLZ=12519)
U 83- 5  F637
U 83- 6  09U2
U 83- 8  883F
U 83- 9  8556
U 83-10  14AP
U 83-11  0000
U 83-12  0000
U 83-13  14AP
U 84- 1  high
U 84- 2  0000
U 84- 3  383A
(TOTLZ=0024)
U 84- 4  high
U 84- 5  0000
U 84- 6  383A
U 84- 8  low
U 84- 9  high
U 84-10  high
U 84-11  0000
U 84-12  high
U 84-13  high
U 88- 1  low
U 88- 2  high
U 88- 4  low
U 88- 6  383A
U 88- 8  C383
U 88- 9  09U2
U 88-10  7A57
U 88-11  low
U 88-12  U352
U 88-13  FC68
U 89- 1  low
U 89- 2  low
U 89- 4  low
U 89- 5  low
U 89- 8  low
U 89-11  low
U 90- 4  low
U 90- 5  high
U 90- 6  high
U 90- 7  low
U 90- 9  low
U 90-10  low
```

```
U 90-11  low
U 90-12  high
U 90-14  high
U 90-15  high
U 91- 6  high
U 91- 7  high
U 91- 9  high
U 91-10  high
U 91-11  high
U 91-12  high
U 91-13  high
U 91-14  high
U 91-15  high
U 92- 1  high
U 92- 2  high
U 92- 5  low
U 92- 7  low
U 92- 9  high
U 92-10  low
U 92-12  high
U 92-15  high
U 93- 1  high
U 93- 2  low
U 93- 5  low
U 93- 7  low
U 93- 9  high
U 93-10  high
U 93-12  high
U 93-15  high
U 94- 1  high
U 94- 2  0000
(TOTLZ=12519)
U 94- 3  high
U 94- 4  low
U 94- 5  low
U 94- 6  low
U 94- 7  high
U 94- 9  383A
(TOTLZ=0024)
U 94-10  high
U 94-11  UPF6
U 94-12  12A9
U 94-13  580H
U 94-14  P816
U 94-15  898A
U 95- 1  high
U 95- 2  0000
(TOTLZ=12519)
U 95- 3  high
U 95- 4  high
U 95- 5  low
U 95- 6  low
U 95- 7  high
U 95- 9  383A
(TOTLZ=0024)
U 95-10  898A
U 95-11  5AFC
U 95-12  5632
U 95-13  82PU
U 95-14  8779
U 95-15  1166
U 96- 1  high
U 96- 2  383A
(TOTLZ=0024)
U 96- 3  low
U 96- 4  high
U 96- 5  high
U 96- 6  high
U 96- 7  high
U 96- 9  383A
(TOTLZ=0001)
U 96-10  U352
U 96-11  4CP2
U 96-12  HU2A
U 96-13  4521
U 96-14  986C
U 96-15  CC34
U 97- 1  AU47
U 97- 2  87AA
U 97- 3  P74A
U 97- 4  4AA4
U 97- 5  AU47
U 97- 6  C126
U 97- 8  C126
U 97- 9  0U22
U 97-10  0000
U 97-11  968U
U 97-12  APC5
U 97-13  383A
(TOTLZ=12518)
U 98- 1  high
U 98- 2  AU47
U 98- 3  977H
U 98- 4  7A57
U 98- 5  4AA4
U 98- 6  729P
U 98- 7  4AA4
U 98- 9  383A
(TOTLZ=25037)
U 98-10  87AA
U 98-11  CU90
U 98-12  87AA
U 98-13  968U
U 98-14  0000
U 98-15  383A
U 99- 1  383A
(TOTLZ=0001)
U 99- 2  383A
(TOTLZ=0025)
U 99- 3  14AP
U 99- 4  5H6A
U 99- 5  5H6A
U 99- 6  5H6A
U 99- 8  87AA
U 99- 9  6UH0
U 99-10  6UH0
U 99-11  4AA4
U 99-12  383A
(TOTLZ=0001)
U 99-13  high
U100- 1  high
U100- 2  A424
U100- 3  0000
(TOTLZ=12519)
U100- 4  high
U100- 5  31F8
U100- 6  09U2
U100- 8  UP0H
U100- 9  F637
U100-10  high
U100-11  0000
(TOTLZ=12519)
U100-12  1716
U100-13  high
U101- 1  383A
U101- 2  0000
U101- 4  low
U101- 5  0000
(TOTLZ=25038)
U101- 6  383A
(TOTLZ=25037)
U101-10  low
U101-11  high
U101-12  high
U101-13  low
```

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section describes adjustments and checks required to return the instrument to peak operating capability after repairs have been made.

5-3. SAFETY REQUIREMENTS.

5-4. Although this instrument has been designed in accordance with international safety standards, general safety precautions must be observed during all phases of operation, service, and repair of the instrument. Failure to comply with precautions listed in the Safety Summary at the front of this manual or with specific warnings given throughout the manual could result in serious injury or death or damage to equipment. Service adjustments should be performed only by qualified service personnel.

5-5. EQUIPMENT REQUIRED.

5-6. HP 64000 series mainframe.
2 HP 64602-66501 200MHz Data Acq. Boards.
2 HP 64604A Timing Probes
2 HP 64604-61601 Timing Cables.
HP 1722B Scope or equivalent.
HP 5314A Universal Counter or equivalent.
HP 10017 Probe or equivalent.
BNC Coaxial Cable approx. 1 meter long.
Alignment Tool.
Small Screwdriver.
HP 64110-66503 Extender Board. (Part of 64934A Service Kit)
4 Extended coaxial clock cables. (Part of 64934B Service Kit)
HP 3-way extended timing bus cable. (Part of 64934B Service Kit)

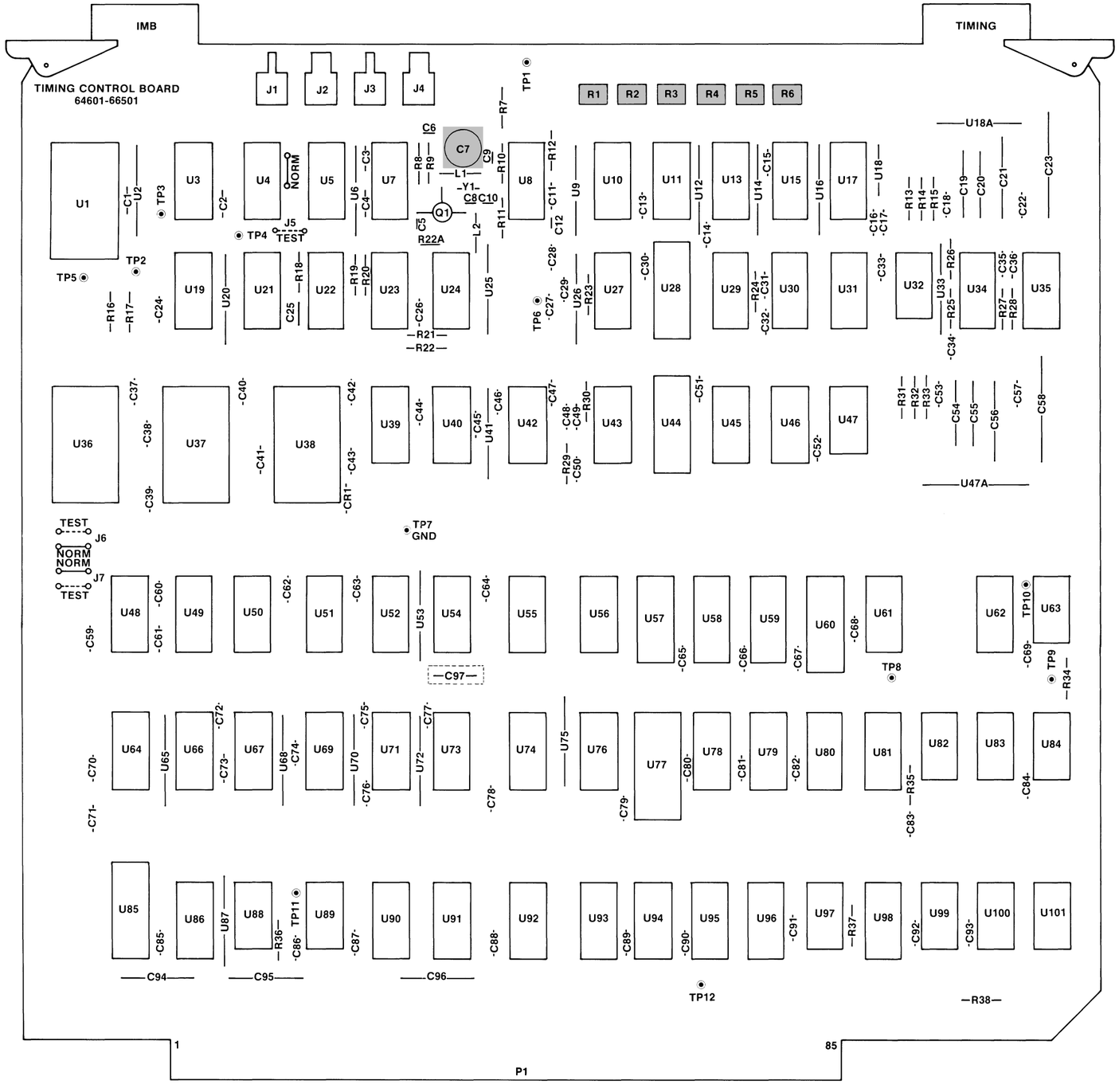

Figure 5-1. Adjustments

5-7. SAMPLE-RATE OSCILLATOR CALIBRATION.

5-8. Setup.

5-9. TP1, the coaxial testpoint for the oscillator, is located at the very top-center of the board (when viewing from the component side). The oscillator transistor (Q1), and its trimmer capacitor (C7), are located at the top of the board between U7 and U8. See figure 5-1.

5-10. Using the mainframe keyboard and softkeys configure the timing analyzer for the oscillator adjustment as follows:

a. Press softkey "timing", then [RETURN]. The screen should show the trace specification.

b. Verify that the "mode_is wide_sample", and the "sample rate_is 200 MHz".

c. Press the softkeys "trigger on entering POD1.0 = 0XXH". [RETURN]

d. Press "execute". [RETURN]

5-11. Adjustment

a. Connect the probe to the 64602A acquisition board through the timing cable. Leave the probe leads disconnected.

b. Connect channel A of the scope to testpoint 1. Since this is a coaxial test point, no ground clip is necessary.

c. Set up CHANNEL A VOLTS/DIV to .01 (100mv/div. with the X10 probe), and AC couple the input.

d. Set up HORIZ DISPLAY to MAG X10 and MAIN.

e. Set up TIME/DIV to 10ns/div. (This is actually 1ns/div., since MAG X10 has been selected).

f. If no signal is present adjust the trimmer capacitor on the upper middle part of the board until a sinusoidal signal is observed (try to adjust the capacitor to the middle of the range when the sinusoid is observed). NOTE: USE A NON-CONDUCTIVE ALIGNMENT TOOL ONLY!!! (ISOLATION IS REQUIRED).

g. The sinusoidal waveform should have an amplitude of 100 to 150mV and a frequency of 200MHz (2 periods/screen on 1ns/div.).

SAMPLE RATE OSCILLATOR CALIBRATION (continued)

h. To determine if the oscillator is stable, tap the collector of the high frequency transistor lightly with the blade of a small screwdriver to see if the oscillator will come back to a stable 200MHz oscillation.

```
                                |
HIGH FREQUENCY TRANSISTOR: --0-|-   <------collector
(located below the trimmer cap.)
```

i. If the oscillator will not come back with the correct oscillation, readjust the trimmer capacitor and repeat the last step to ensure a stable oscillation.

j. Connect the scope probe BNC to INPUT A of the 5314A Universal Counter. Set up the counter for NORM FREQ A 10Hz RESOLUTION positive SLOPE ATTN X1 and adjust LEVELA on the counter to approximately the middle position.

k. Connect the scope probe tip to TP4 (located between U4 and U20) , and connect the ground lead of the scope probe to TP7 (GND).

l. The counter should display 50MHz +/- 0.01% (49995kHz - 50005kHz).

Press softkey "end". Press [RETURN].

5-12. TRIGGER DURATION CALIBRATION (R1 through R6)

5-13. Besides the previous sample rate oscillator adjustment, there are six adjustments for trigger duration on the 64601A control board. The six pots, R1-R6, are located at the top of the board (when viewed from the component side). The last three adjustments, R4-R6, are for a 16-channel, two-acquisition board system ONLY.

5-14. The duration pots, R1-R6 at the top of the 64601A control board, determine the pattern duration required for triggering.

5-15. Use PV tests 6 and 10 for adjustment of R1 through R6. For an 8-channel single acquisition board system, only R1, R2, and R3 need to be adjusted.

5-16. A slight readjustment may be necessary whenever the 64601A control board is moved to a different mainframe.

5-17. Hardware Setup.

a. Connect the timing probes to the data acquisition boards through the timing cables.

b. Disconnect all channels from any signal source: that is, leave the probes disconnected.

5-18. 8-Channel Keyboard Setup. Use the following procedure to adjust R1-R3.

a. Press softkey "option_test". [RETURN]

b. The screen should list all the option boards installed in your system. Type in the slot number for the 64601A control board. [RETURN]

c. Press softkey "run".

d. Press softkey "slot".

e. The screen should list the timing analyzer boards in the system. Type in the slot number for the 64601A control board.

f. Press softkey "test". The screen should list all the Control Board PV tests.

g. Type in "6".

h. Type in "cal". [RETURN]

5-19. 8-Channel Adjustment. (R1 through R3)

Test 6 consists of nine test steps, five in braces, and four in brackets: {00000}[0000]. We are concerned only with the four in brackets. All four should be 0. If they are not, procede as follows:

1. Adjust R1 until the second digit from the right is 0.
2. Adjust R2 until the third digit from the right is 0.
3. Adjust R3 until the fourth digit from the right is 0.
4. The first bracket digit indicates whether the others are correct. It should now be 0 also.
5. Press the "stop" softkey.
6. Press the "end" softkey.

5-20. 16-Channel Keyboard Setup. (R4 through R6)

Use the following procedure to adjust R4-R6 in a system containing a second 64602A acquisition board.

a. Press softkey "option_test". [RETURN]

b. The screen should list all the option boards installed in your system. Type in the slot number for the 64601A control board. [RETURN]

c. Press softkey "run".

d. Press softkey "slot".

e. The screen should list the timing analyzer boards in the system. Type in the slot number for the 64601A control board.

f. Press softkey "test".

g. The screen should list the 15 control board PV tests. Type in "10".

h. Type in "cal". [RETURN]

5-21. 16-channel adjustment procedure. (R4 through R6)

When test 10 is displayed, nine digits are shown: five in braces, and four in brackets. We are concerned only with the four bracket digits. The four digits in brackets should all be 0. If they are not, procede as follows:

1. Adjust R4 until the second digit from the right is 0.
2. Adjust R5 until the third digit from the right is 0.
3. Adjust R6 until the fourth digit from the right is 0.
4. The first digit from the right should be 0 when the other three are 0.
5. Press the "stop" softkey. [RETURN]
6. Press the "end" softkey. [RETURN].

NOTES

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five-digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used: one all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Chassis-mounted parts in alphanumerical order by reference designation.

b. Electrical assemblies and their components in alphanumerical order by reference designation.

c. Miscellaneous parts.

The information given for each part consists of the following:

a. The Hewlett-Packard part number and the check digit.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A five-digit code that indicates the manufacturer.

e. The manufacturer's part number.

The total quantity for each part is given only once--at the first appearance of the part number in the list.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the replaceable parts table, quote the Hewlewtt-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-9. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-10. SPARE PARTS KIT.

6-11. A service kit is available. To order, please contact your local sales and service representative.

6-12. DIRECT MAIL ORDER SYSTEM.

6-13. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP Parts Center in Mountain View California.

b. No Maximum or minimum on any mail order (there is a minimum order amount, for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (A small handling charge for each order).

d. No invoices--to provide these advantages, a check or money order must accompany each order.

6-14. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	spring
COEF	= coeficient			**OX**	oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	micro = 10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	without

Table 6-2. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64601A	9	1	TIMING ANALYSIS CONTROL BOARD	28480	64601A
A1	64601-66502	2	1	TIMING CONTROL BOARD	28480	64601-66502
A1C1	0160-2055	9	65	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C2	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C5	0160-3879	7	3	CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C6	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C7	0121-0061	1	1	CAPACITOR-V TRMR-CER 5.5-18PF 350V	52763	304322 5.5/18PF NPO
A1C8	0160-4383	0	1	CAPACITOR-FXD 6.8PF +-.5PF 200VDC CER	20932	5024E0200RD689D
A1C9	0160-3874	2	6	CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A1C10	0160-3874	2	4	CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A1C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C12	0160-3879	7		CAPACITOR-FXD .01UF +-20% 100VDC CER	28480	0160-3879
A1C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C15	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C18	0140-0199	6	2	CAPACITOR-FXD 240PF +-5% 300VDC MICA	72136	DM15F241J0300WV1CR
A1C19	0160-5415	1	2	CAPACITOR-FXD 3600PF 50VDC	28480	0160-5415
A1C20	0160-5343	4	2	CAPACITOR-FXD .04UF 50VDC	28480	0160-5343
A1C21	0160-5342	3	2	CAPACITOR-FXD .4UF 50VDC	28480	0160-5342
A1C22	0160-3874	2		CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A1C23	0160-5341	2	2	CAPACITOR-FXD 4UF 50VDC	28480	0160-5341
A1C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C27	0160-3875	3	2	CAPACITOR-FXD 22PF +-.5PF 200VDC CER	28480	0160-3875
A1C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C29	0160-4813	1	3	CAPACITOR-FXD 180PF +-5% 100VDC CER	28480	0160-4813
A1C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C32	0160-4492	2	2	CAPACITOR-FXD 18PF +-5% 200VDC CER 0+-30	28480	0160-4492
A1C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C35	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C36	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C37	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C38	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C39	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C40	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C41	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C42	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C43	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C44	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C45	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C46	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C47	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C48	0160-4813	1		CAPACITOR-FXD 180PF +-5% 100VDC CER	28480	0160-4813
A1C49	0160-3875	3		CAPACITOR-FXD 22PF +-.5PF 200VDC CER	28480	0160-3875
A1C50	0160-4492	2		CAPACITOR-FXD 18PF +-5% 200VDC CER 0+-30	28480	0160-4492
A1C51	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C52	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C53	0140-0199	6		CAPACITOR-FXD 240PF +-5% 300VDC MICA	72136	DM15F241J0300WV1CR
A1C54	0160-5415	1		CAPACITOR-FXD 3600PF 50VDC	28480	0160-5415
A1C55	0160-5343	4		CAPACITOR-FXD .04UF 50VDC	28480	0160-5343
A1C56	0160-5342	3		CAPACITOR-FXD .4UF 50VDC	28480	0160-5342
A1C57	0160-3874	2		CAPACITOR-FXD 10PF +-.5PF 200VDC CER	28480	0160-3874
A1C58	0160-5341	2		CAPACITOR-FXD 4UF 50VDC	28480	0160-5341
A1C59	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C60	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C61	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C62	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C63	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C64	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C65	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C66	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C67	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C68	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C69	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C70	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1C71	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C72	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C73	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C74	0160-4813	1		CAPACITOR-FXD 180PF +-5% 100VDC CER	28480	0160-4813
A1C75	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C76	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C77	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C78	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C79	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C80	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C81	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C82	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C83	0140-0198	5	1	CAPACITOR-FXD 200PF +-5% 300VDC MICA	72136	DM15F201J0300WV1CR
A1C84	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C85	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C86	0160-4808	4	1	CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
A1C87	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C88	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C89	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C90	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C91	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C92	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C93	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C94	0180-0374	3	3	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A1C95	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A1C96	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
A1C97	0160-4822	2	1	CAPACITOR-FXD 1000 PF +-5% 100 VDC CER	28480	0160-4822
A1C98	0160-3569	2	1	CAPACITOR-FXD 27PF +-5% 200VDC CER	28480	0160-3569
A1CR1	1901-0040	1	1	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1J1	1250-0543	8	2	CONNECTOR-RF SM-SNP M PC 50-OHM	28480	1250-0543
A1J2	1250-1189	0	2	CONNECTOR-RF SMB FEM PC 50-OHM	28480	1250-1189
A1J3	1250-0543	8		CONNECTOR-RF SM-SNP M PC 50-OHM	28480	1250-0543
A1J4	1250-1189	0		CONNECTOR-RF SMB FEM PC 50-OHM	28480	1250-1189
A1L1	9100-2247	4	1	INDUCTOR RF-CH-MLD 100NH 10% .105DX.26LG	28480	9100-2247
A1L2	9100-2248	5	1	INDUCTOR RF-CH-MLD 120NH 10% .105DX.26LG	28480	9100-2248
A1MP1	1480-0116	8	1	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
A1MP2	64601-85001	6	1	BOARD EJECTOR	28480	64601-85001
A1MP3	64601-85002	7	1	BOARD EJECTOR	28480	64601-85002
A1P1	1258-0182	7	3	CONNECTOR-R & P 1 MALE PLUG	28480	1258-0182
A1P2	1258-0182	7		CONNECTOR-R & P 1 MALE PLUG	28480	1258-0182
A1P3	1258-0182	7		CONNECTOR-R & P 1 MALE PLUG	28480	1258-0182
A1Q1	1854-0591	6	1	TRANSISTOR NPN SI PD=180MW FT=4GHZ	25403	BFR-90
A1R1	2100-3352	7	4	RESISTOR-TRMR 1K 10% C SIDE-ADJ 1-TRN	28480	2100-3352
A1R2	2100-3352	7		RESISTOR-TRMR 1K 10% C SIDE-ADJ 1-TRN	28480	2100-3352
A1R3	2100-3351	6	2	RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
A1R4	2100-3352	7		RESISTOR-TRMR 1K 10% C SIDE-ADJ 1-TRN	28480	2100-3352
A1R5	2100-3352	7		RESISTOR-TRMR 1K 10% C SIDE-ADJ 1-TRN	28480	2100-3352
A1R6	2100-3351	6		RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	28480	2100-3351
A1R7	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R8	0757-0401	0	3	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R9	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R10	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R11	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R12	0757-0410	1	1	RESISTOR 301 1% .125W F TC=0+-100	24546	C4-1/8-T0-301R-F
A1R13	0757-0426	9	2	RESISTOR 1.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1301-F
A1R14	0757-0427	0	2	RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A1R15	0757-0414	5	2	RESISTOR 432 1% .125W F TC=0+-100	24546	C4-1/8-T0-432R-F
A1R16	0698-3132	4	1	RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A1R17	0757-0405	4	1	RESISTOR 162 1% .125W F TC=0+-100	24546	C4-1/8-T0-162R-F
A1R18	0757-0391	7	6	RESISTOR 39.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-39R2-F
A1R19	0757-0391	7		RESISTOR 39.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-39R2-F
A1R20	0757-0391	7		RESISTOR 39.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-39R2-F

See introduction to this section for ordering information
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Table 6-2. Replaceable Parts List (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R21	0757-0391	7		RESISTOR 39.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-39R2-F
A1R22	0757-0391	7		RESISTOR 39.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-39R2-F
A1R22A	0757-0391	7		RESISTOR 39.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-39R2-F
A1R23	0757-0407	6	5	RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A1R24	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A1R25	0757-0416	7	5	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A1R26	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A1R27	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A1R28	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A1R29	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A1R30	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A1R31	0757-0426	9		RESISTOR 1.3K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1301-F
A1R32	0757-0427	0		RESISTOR 1.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1501-F
A1R33	0757-0414	5		RESISTOR 432 1% .125W F TC=0+-100	24546	C4-1/8-T0-432R-F
A1R34	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R35	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1R36	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A1R37	0757-0407	6		RESISTOR 200 1% .125W F TC=0+-100	24546	C4-1/8-T0-201-F
A1R38	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1TP1	1250-1737	4	1	COAXIAL TEST POINT	28480	1250-1737
A1TP2	0360-0535	0	11	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP10	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP11	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1TP12	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A1U1	1NB4-5008	9	4	IC-DELAY	28480	1NB4-5008
A1U2	1810-0273	9	1	NETWORK-RES 10-SIP470.0 OHM X 9	01121	210A471
A1U3	1820-2359	7	1	IC MISC ECL 14-INP	07263	F10014PC
A1U4	1820-1359	5	1	IC MUXR/DATA-SEL ECL 4-TO-1-LINE DUAL	04713	MC10174P
A1U5	1820-1225	4	3	IC FF ECL D-M/S DUAL	04713	MC10231P
A1U6	1810-0271	7	9	NETWORK-RES 10-SIP200.0 OHM X 9	01121	210A201
A1U7	1820-1320	0	2	IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10216L
A1U8	1820-0920	4	1	IC RCVR ECL LINE RCVR QUAD 2-INP	04713	MC1692L
A1U9	1810-0272	8	7	NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A1U10	1820-2193	7	5	IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176L
A1U11	1820-2193	7		IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176L
A1U12	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A1U13	1820-0815	6	3	IC GATE ECL AND-OR	04713	MC10121P
A1U14	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A1U15	1820-2193	7		IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176L
A1U16	1810-0271	7		NETWORK-RES 10-SIP200.0 OHM X 9	01121	210A201
A1U17	1820-0815	6		IC GATE ECL AND-OR	04713	MC10121P
A1U18A	1810-0281	9	2	NETWORK-RES 10-SIP100.0K OHM X 9	01121	210A104
A1U18	1810-0541	4	1	NETWORK-RES 6-SIP MULTI-VALUE	28480	1810-0541
A1U19	1820-0802	1	6	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A1U20	1810-0271	7		NETWORK-RES 10-SIP200.0 OHM X 9	01121	210A201
A1U21	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A1U22	1820-2664	7	1	IC CNTR ECL BI-QUINARY R-S POS-EDGE-TRIG	04713	MC1678L
A1U23	1820-1225	4		IC FF ECL D-M/S DUAL	04713	MC10231P
A1U24	1820-0796	2	1	IC GATE ECL NOR QUAD 2-INP	04713	MC1662L
A1U25	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A1U26	1810-0271	7		NETWORK-RES 10-SIP200.0 OHM X 9	01121	210A201
A1U27	1820-0802	1	6	IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A1U28	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A1U29	1810-0402	6	2	NETWORK-RES 16-DIP330.0 OHM X 8	01121	316B331
A1U30	1810-0243	3	1	NETWORK-RES 16-DIP6.8K OHM X 8	01121	316B682
A1U31	1858-0054	4	2	TRANSISTOR ARRAY 16-PIN PLSTC DIP	28480	1858-0054
A1U32	1821-0002	5	2	TRANSISTOR ARRAY 14-PIN CER DIP	3L585	CA3045
A1U33	1810-0271	7		NETWORK-RES 10-SIP200.0 OHM X 9	01121	210A201
A1U34	1820-1320	0		IC RCVR ECL LINE RCVR TPL 2-INP	04713	MC10216L
A1U35	1820-1946	6	3	IC GATE ECL DUAL	04713	MC10117L
A1U36	1NB4-5008	9		IC-DELAY	28480	1NB4-5008
A1U37	1NB4-5008	9		IC-DELAY	28480	1NB4-5008
A1U38	1NB4-5008	9		IC-DELAY	28480	1NB4-5008
A1U39	1820-1993	3	1	IC MUXR/DATA-SEL ECL QUAD 2-INP	04713	MC10158L
A1U40	1820-1225	4		IC FF ECL D-M/S DUAL	04713	MC10231P
A1U41	1810-0271	7		NETWORK-RES 10-SIP200.0 OHM X 9	01121	210A201
A1U42	1820-1946	6		IC GATE ECL DUAL	04713	MC10117L
A1U43	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A1U44	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
A1U45	1810-0402	6		NETWORK-RES 16-DIP330.0 OHM X 8	01121	316B331

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Table 6-2. Replaceable Parts List (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U46	1858-0054	4		TRANSISTOR ARRAY 16-PIN PLSTC DIP	28480	1858-0054
A1U47A	1810-0281	9		NETWORK-RES 10-SIP100.0K OHM X 9	01121	210A104
A1U47	1821-0002	5		TRANSISTOR ARRAY 14-PIN CER DIP	3L585	CA3045
A1U48	1820-0780	4	1	IC DRVR TTL LINE DRVR QUAD	27014	DS8831N
A1U49	1820-1052	5	2	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U50	1820-1946	6		IC GATE ECL DUAL	04713	MC10117L
A1U51	1820-0817	8	2	IC FF ECL D-M/S DUAL	04713	MC10131P
A1U52	1820-1788	4	1	IC CNTR ECL BIN SYNCHRO POS-EDGE-TRIG	07263	F10016DC
A1U53	1810-0271	7		NETWORK-RES 10-SIP200.0 OHM X 9	01121	210A201
A1U54	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A1U55	1820-0815	6		IC GATE ECL AND-OR	04713	MC10121P
A1U56	1820-1196	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A1U57	1818-1596	7	3	IC CMOS 4096 (4K) STAT RAM 55-NS 3-S	S4013	HM6147P-3
A1U58	1818-1596	7		IC CMOS 4096 (4K) STAT RAM 55-NS 3-S	S4013	HM6147P-3
A1U59	1818-1596	7		IC CMOS 4096 (4K) STAT RAM 55-NS 3-S	S4013	HM6147P-3
A1U60	1820-1677	0	1	IC FF TTL S D-TYPE OCTL	01295	SN74S374N
A1U61	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A1U62	1820-1077	4	1	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
A1U63	1820-0693	8	3	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U64	1820-1052	5		IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
A1U65	1810-0271	7		NETWORK-RES 10-SIP200.0 OHM X 9	01121	210A201
A1U66	1820-1944	4	1	IC LCH ECL D-TYPE POS-EDGE-TRIG DUAL	04713	MC10130L
A1U67	1820-0802	1		IC GATE ECL NOR QUAD 2-INP	04713	MC10102P
A1U68	1810-0271	7		NETWORK-RES 10-SIP200.0 OHM X 9	01121	210A201
A1U69	1820-1400	7	1	IC GATE ECL AND QUAD 2-INP	04713	MC10104P
A1U70	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A1U71	1820-2193	7		IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176L
A1U72	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A1U73	1820-2193	7		IC FF ECL D-M/S POS-EDGE-TRIG COM CLOCK	04713	MC10176L
A1U74	1820-0817	8		IC FF ECL D-M/S DUAL	04713	MC10131P
A1U75	1810-0280	8	1	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
A1U76	1820-1641	8	1	IC DRVR TTL LS BUS DRVR HEX 1-INP	01295	SN74LS365AN
A1U77	1816-1308	5	1	IC TTL L 1024 (1K) STAT RAM 75-NS 3-S	07263	93L422PC
A1U78	1820-1430	3	2	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U79	64601-10002	0	1	IC-7611A- 5-FORMAT	28480	64601-10002
A1U80	64601-10001	9	1	ROM-PROGRAMMED 5-CHAR	28480	64601-10001
A1U81	1820-1076	3	1	IC FF TTL S D-TYPE POS-EDGE-TRIG CLEAR	01295	SN74S174N
A1U82	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U83	1820-1158	2	1	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
A1U84	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U85	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
A1U86	1820-1173	1	1	IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
A1U87	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
A1U88	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A1U89	1820-0269	4	1	IC GATE TTL NAND QUAD 2-INP	01295	SN7403N
A1U90	1820-2799	9	1	IC-SN74LS259	28480	1820-2799
A1U91	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U92	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A1U93	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A1U94	1820-1475	6	2	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U95	1820-1475	6		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	07263	93S16DC
A1U96	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
A1U97	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
A1U98	1820-1191	3	1	IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
A1U99	1820-0686	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
A1U100	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U101	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
A1XU1	1200-0541	1	4	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A1XU13	1200-0607	0	22	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU17	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU19	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU21	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU22	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU28	1200-0639	8	3	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU31	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU32	1200-0638	7	7	SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1XU36	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A1XU37	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A1XU38	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A1XU44	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU46	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU47	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1XU48	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU54	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU55	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU56	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU57	1200-0539	7	3	SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts List (Con't)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1XU58	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
A1XU59	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
A1XU76	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU77	1200-0612	7	1	SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
A1XU78	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU79	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU80	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU84	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1XU85	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU88	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1XU89	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1XU90	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU91	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU92	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU93	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU94	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU95	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU96	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
A1XU97	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1XU101	1200-0638	7		SOCKET-IC 14-CONT DIP DIP-SLDR	28480	1200-0638
A1Y1	0410-1335	7	1	CRYSTAL-200MC	28480	0410-1335
W1	8120-4094	4	1	CABLE TIMING-2 CONNECTOR	28480	8120-4094
W2	8120-4093	3	1	CABLE TIMING-3 CONNECTOR	28480	8120-4093
W3	64620-61620	8	1	CABLE-ASYNCHRONOUS INTER-MODULE	28480	64620-61620

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
S0167	FUJITSU LTD	TOKYO	JP	
S4013	HITACHI	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND	CA	91745
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
11236	CTS OF BERNE INC	BERNE	IN	46711
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
20932	EMCON DIV ITW	SAN DIEGO	CA	92129
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
25403	AMPEREX ELEK CORP SEMICON & MC DIV	SLATERSVILLE	RI	02876
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
27167	CORNING GLASS WORKS (WILMINGTON)	WILMINGTON	NC	28401
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
52763	STETTNER-TRUSH INC	CAZENOVIA	NY	13035
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP	FLORENCE	SC	06226
75042	TRW INC PHILADELPHIA DIV	PHILADELPHIA	PA	19108

See introduction to this section for ordering information

NOTES

SECTION VII

MANUAL CHANGES

This section normally contains information for backdating this manual for models with repair numbers prior to the one shown on the title page. Because this edition includes the information for the first repair number, there is no backdating material.

NOTES

SECTION VIII

THEORY AND SCHEMATICS

8-1. INTRODUCTION.

8-2. This section contains block diagrams, theory of operation, mnemonic tables, and schematics. Some theory of operation is also given in SECTION 4.

8-3. LOGIC CONVENTION

8-4. Logic states are defined as follows:

0----------False, negated, inactive, or unasserted state.

1----------True, active, or asserted state.

8-5. Voltage levels representing logic states:

LOW (L)--------The more negative of two voltage levels.

HIGH (H)-------The more positive of two voltage levels.

8-6. Signals may be either high true, or low true, as indicated by the mnemonics on the service sheets.

8-7. The 64601A includes both TTL and ECL ICs. Worst case voltage levels for trouble shooting and signature analysis purposes are as follows: (IC data sheet specifications may be better than this).

TTL Voltage Levels		ECL Voltage Levels	
Level	Voltage	Level	Voltage
LOW	<0.8	LOW	<-1.50
HIGH	>2.0	HIGH	>-1.10

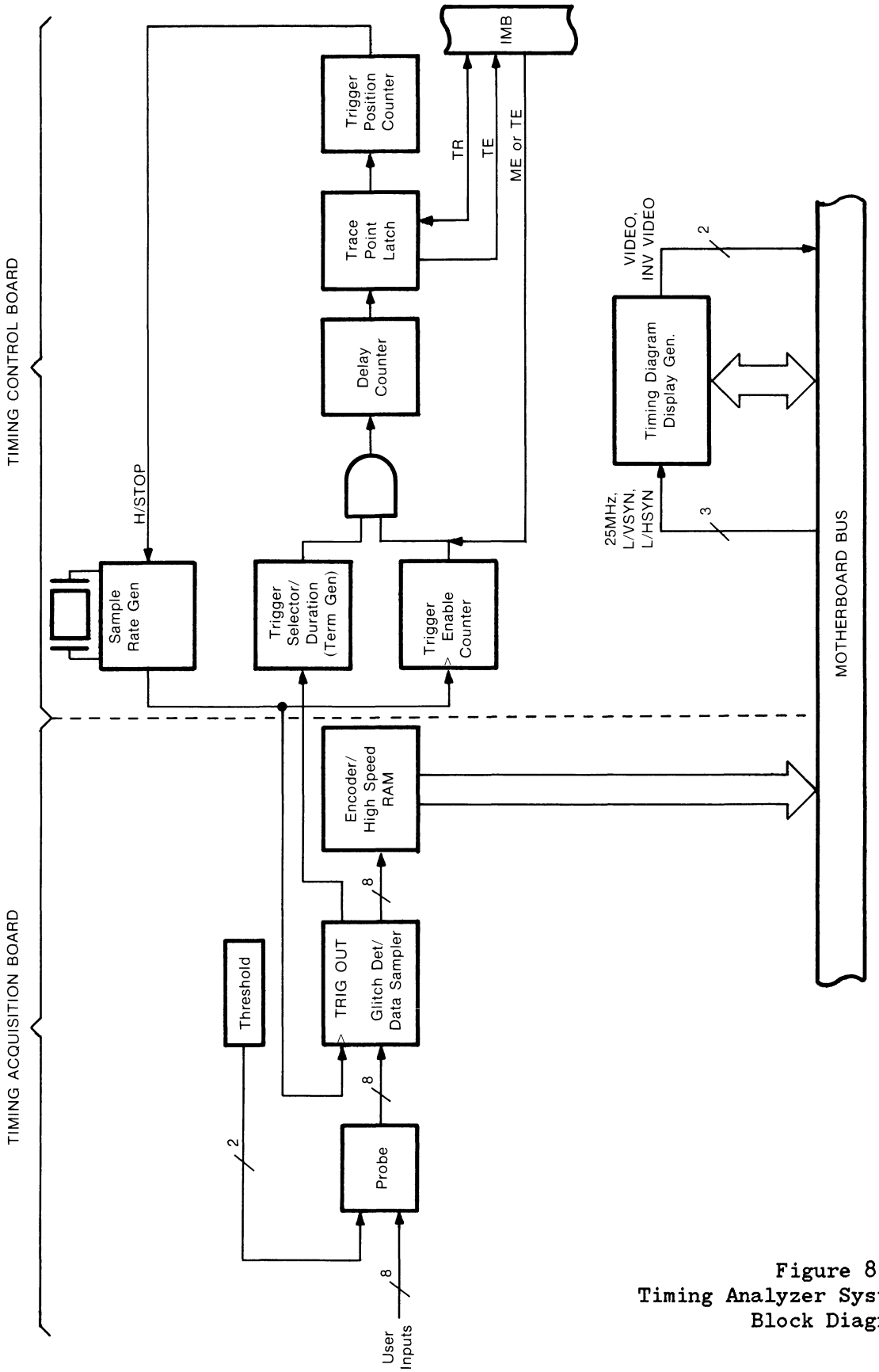


Figure 8-1.
Timing Analyzer System
Block Diagram

8-8. TIMING SYSTEM THEORY. (Fig. 8-1)

8-9. The timing analyzer consists of either two or three boards. In an 8-channel system there is one 8-channel acquisition board and one control board in the next higher mainframe slot. One timing probe is connected to each acquisition board.

8-10. The D/A converters on the acquisition board set the probe thresholds. The upper four channels can be programmed with an upper threshold, and the lower four channels with a lower threshold for dual threshold operation.

8-11. The eight inputs go into the probe, and after conditioning are sent out as 16 differential inputs to the acquisition board. The 16 inputs go into a "glitch" custom IC, along with four sample clocks, which determine the rate at which the acquisition board looks at data from the probe. Except for Glitch Mode, the triggering is asynchronous. The glitch chip's holding register has been programmed with the specified pattern during RESET, and will cause a trigger only when the incoming pattern agrees with the one specified. The glitch chip also looks for glitches in the glitch mode, and will cause a trigger if the glitch occurs at the time specified.

8-12. In a timing analysis system, the incoming data is constantly being stored in memory, regardless of whether a trigger has occurred. The encoders serialize the high-speed data so it may be loaded into low-speed RAM.

8-13. When the glitch chip recognizes that incoming pattern is the same as what was previously programmed into its holding register, it sends a trigger to the control board via the timing bus, which connects the control board to the acquisition board.

8-14. A trigger selector (U13,17) determines which acquisition board signal may become the trigger. Triggers may be ANDed or ORed. Durations or transitions may also be specified. If the trigger signal satisfies the qualifications at this point, and if the trigger has been enabled, either internally, or externally via the IMB from another analyzer, the trigger will be sent on to the delay counter.

8-15. The delay counter (U37) may be programmed to cause a delay from the time a trigger has come out of the glitch chip until the start of an actual trace in memory. Memory is continuously be filled, but "good" data does not occur until tracepoint (trigger + delay) has occurred. The delay counter is clocked internally by the sample clock, or externally from the IMB (DLCK) if the delay must be synchronous.

8-16. The programmable delay counter sends its terminal count to a tracepoint latch (U51). The tracepoint latch may be loaded either by the internal trigger signal, or by a trigger from another analyzer via the IMB.

8-17. The tracepoint signal now goes to the programmable window, or trigger position counter (U36), which determines how much post-tracepoint memory will be filled. The window counter's terminal count stops the sample clock and the memory address counters on the acquisition board. By determining the size of the window between tracepoint and end-of-acquisition, the window counter determines the position of tracepoint in memory.

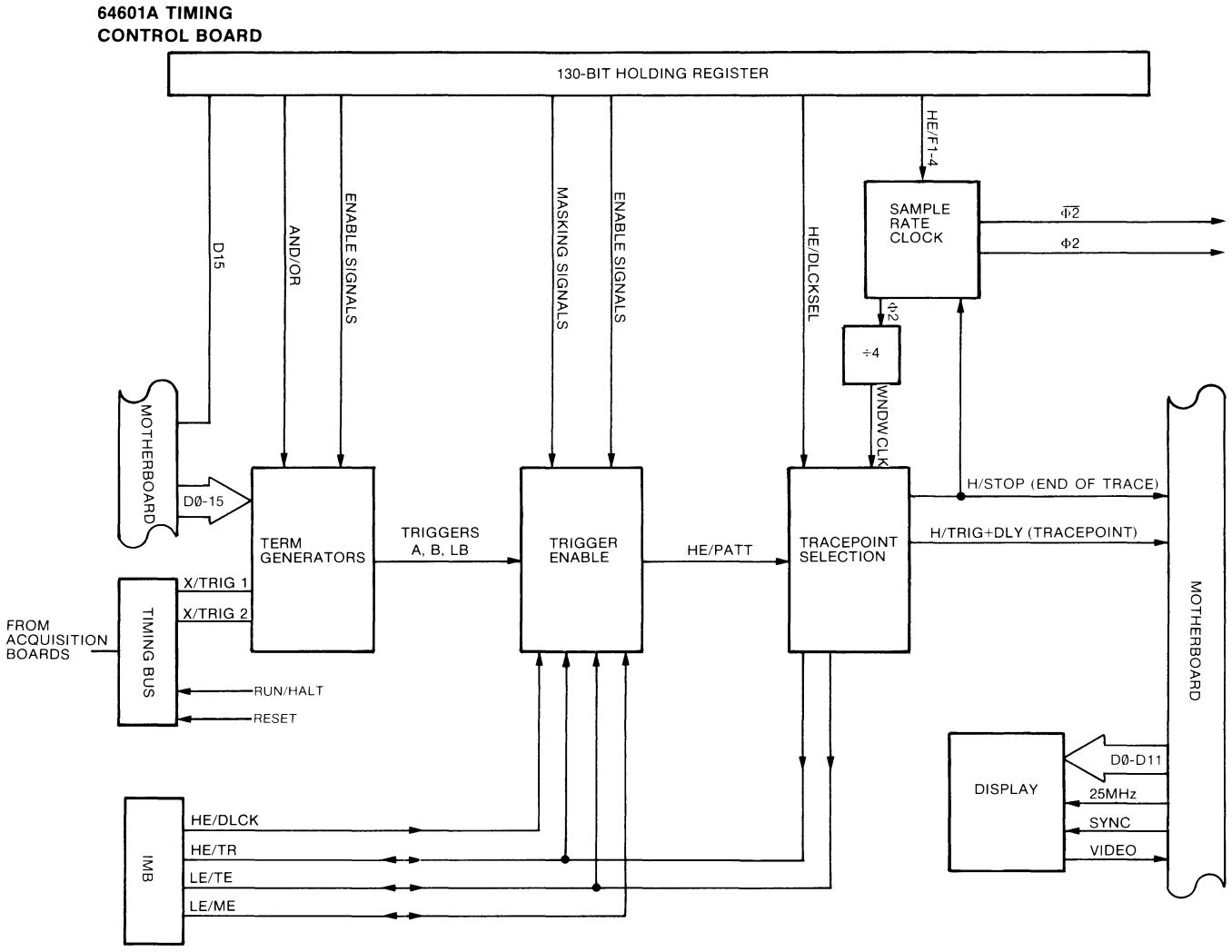


Figure 8-2.
Timing Control Board
Block Diagram

8-18. TIMING CONTROL BOARD THEORY. (Fig. 8-2)

8-19. 130-Bit Control Holding Register.

8-20. The CPU programs the timing analyzer by loading 130 bits into a holding register, consisting of the 25-bit registers in U1, 36, 37, 38, and the 6-bit registers U10, 11, 15, 71, and 73. The analyzer can be programmed to AND or OR triggers from two acquistion boards, sample at different rates up to 400MHz, generate and combine up to two terms, trigger on entering or leaving pattern transitions, trigger on maximum or minimum pattern durations, or delay for specified times after triggering.

8-21. IMB (Inter Module Bus).

8-22. The IMB is the means by which the timing analyzer communicates with other analyzers, such as a state analyzer. The timing analyzer can be clocked, or triggered, or enabled externally. It can also enable, delay, or trigger another analyzer.

8-23. Timing Bus.

8-24. The timing bus is the means by which the control board communicates with one or two timing acquisition boards. The control board sends the acquisition board sample clocks and RESET and RUN commands; the acquisition board(s) sends the control board a trigger signal when the specified pattern is found and memory has been filled.

8-25. Motherboard.

8-26. The motherboard is the mainframe bus which communicates power and CPU programming signals to the timing analyzer.

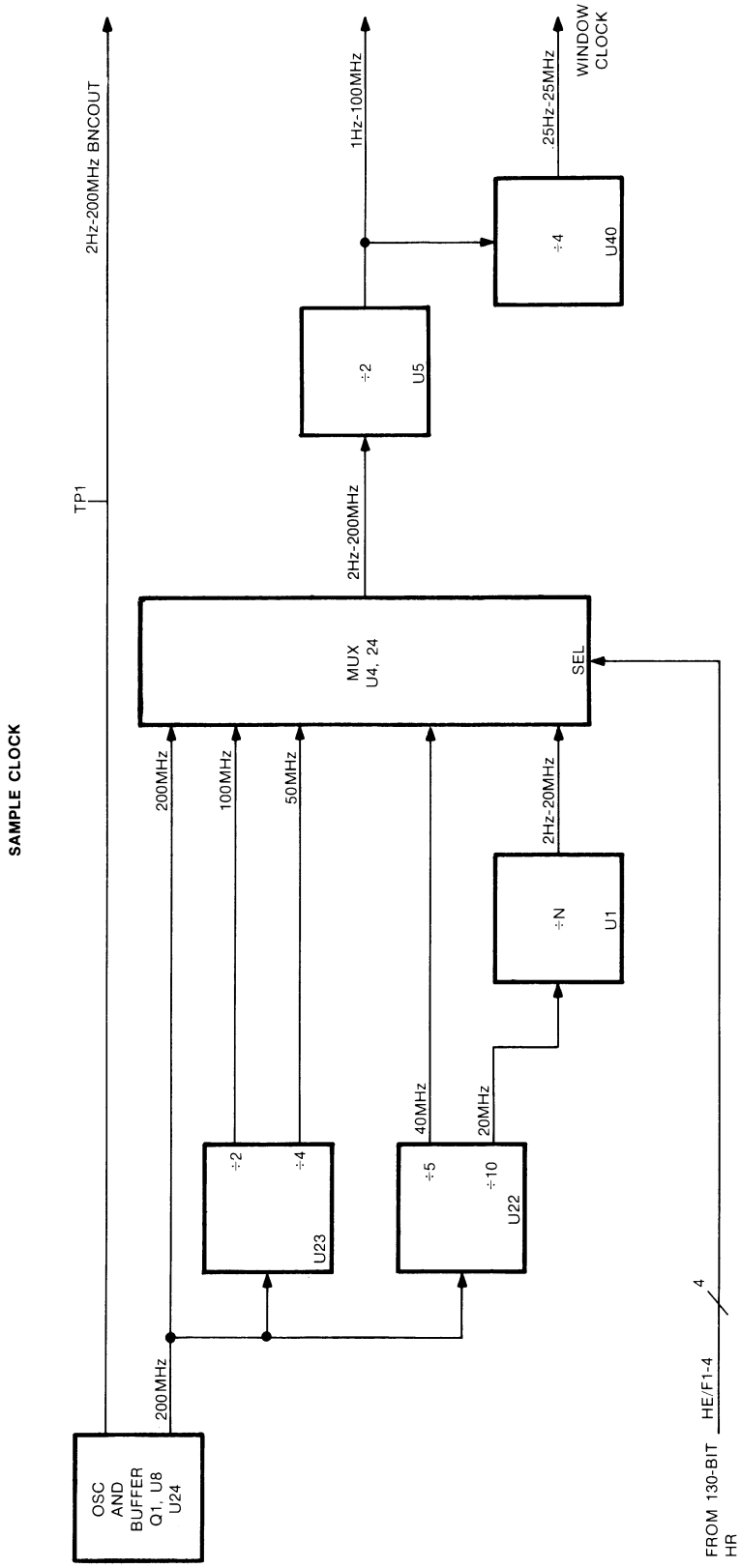
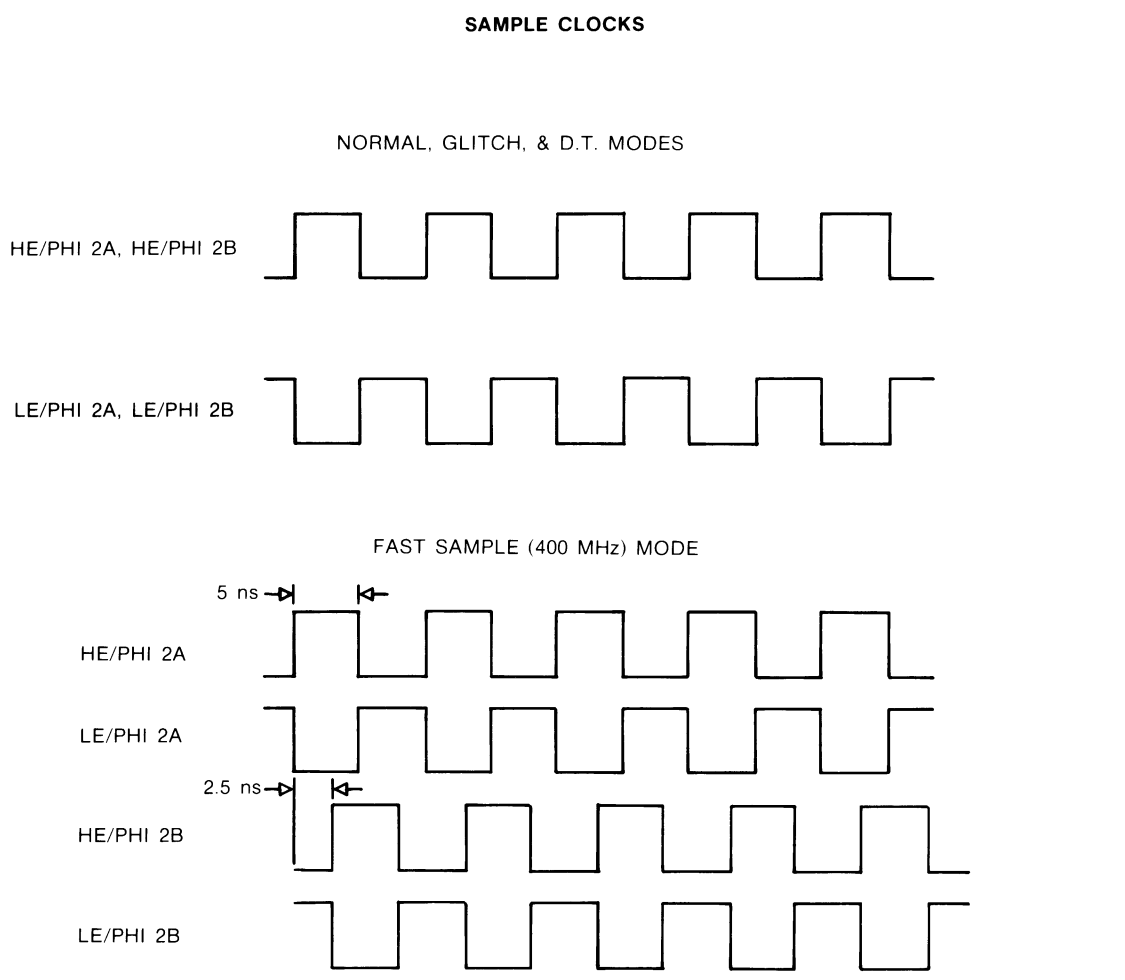


Figure 8-3.
Sample Rate Clock
Block Diagram

8-27. SAMPLE RATE CLOCK THEORY. (Figs. 8-3, 8-10)

8-28. The sample rate clock determines the frequency at which the timing analyzer samples data. The maximum clock frequency is 100MHz, but data is sampled on both clock edges, allowing a maximum sample rate of 200MHz in the Wide Sample Mode.

8-29. In Fast Sample Mode the clock is split into two phases, allowing four edges in the same time period, thus effectively increasing the sample rate to 400MHz. In the Fast Sample Mode the number of channels in an eight channel system is decreased from eight to four, since every second channel is sampled at the second clock phase.



NOTE:
DATA FROM THE PROBE IS SAMPLED ON BOTH THE RISING & FALLING EDGE OF EACH CLOCK SIGNAL.

Figure 8-4. Sample Clock Waveforms

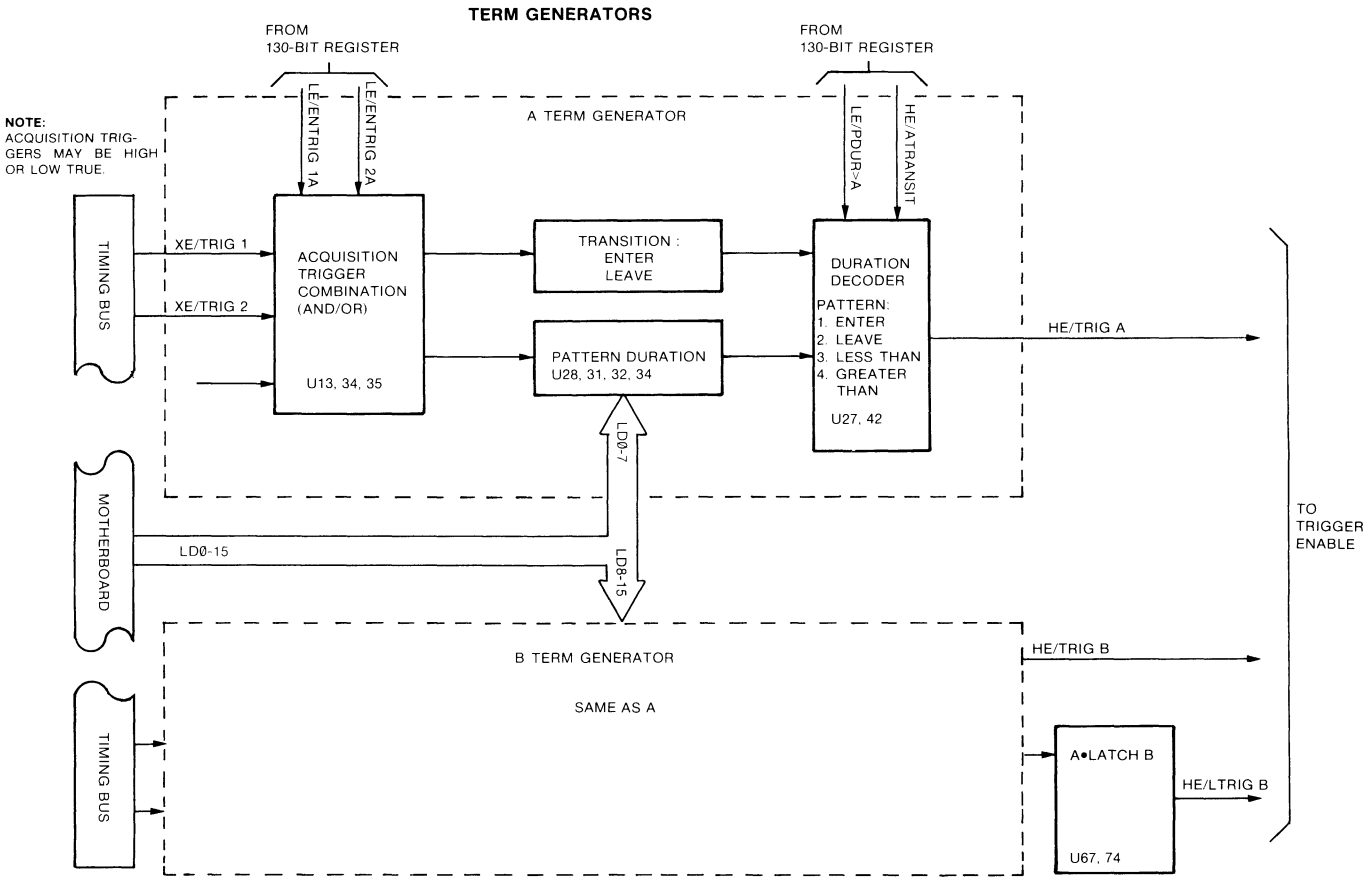


Figure 8-5.
Term Generators
Block Diagram

8-30. TERM GENERATORS. (Figs. 8-4, 8-11, 8-12)

8-31. The term generators receive, combine, and qualify the trigger(s) from the acquisition board(s). There are two term generators, A and B, on a timing control board. Thus, an A trigger, a B trigger, or a B-Latched-Then-A trigger signal may be generated. A and B terms may be ANDed, but the latched-B and B triggers are mutually exclusive.

8-32. The "A" term generator will be described. One of the outputs of the AND/OR trigger combination IC is a ramp moving down toward -5.2V (U35-3). The ramp moves down at a rate determined by the combination of capacitors and current sources turned on by the programming. At some point the ramp will reach the schmitt trigger (U34) threshold. The schmitt will thus trigger sooner or later, depending on the programmed duration.

8-33. The other output of the AND/OR trigger combination IC is a high-going pulse into the transition circuit (U27). One of the paths through U27 is delayed, so that when the pulse finally goes low again, a negative glitch occurs (U27-9).

8-34. When a trigger satisfies the conditions of the "A" term generator, the output (HE/TRIGA at U42-3) is a positive-going pulse. This output can occur under four different conditions:

a. Greater-Than durations: The pattern must last longer than the A term generator specifies.

b. Less-Than durations : The pattern must last less than the A term generator specifies.

c. Leaving transitions : A trigger will occur when the pattern is leaving the specified pattern.

d. Entering transitions : A trigger will occur when the input data is entering the specified pattern.

8-35. Three signals determine which of the above situations will cause an A trigger (HE/TRIGA). Tables for these signals are given on the service sheets for the term generators (4 and 5).

a. XE/TRIG1 and XE/TRIG2 from the acquisition boards may be programmed to be either high true, or low true, at the output of the glitch chip. These signals are programmed low for entering transitions. For all other situations, they are high true.

b. LE/PDUR>A (pattern duration greater than A specifies) is low, or true, only for greater-than durations.

c. HE/TRANSITA is high, or true, only when transitions are specified.

8-36. In the B term generator, there is a latched B circuit, which allows a B trigger to be latched. Then, if an A trigger occurs afterwards, HE/LTRIGB will be true out of the B term generator. The latched-B trigger is mutually exclusive with the normal B trigger signal, HE/TRIGB.

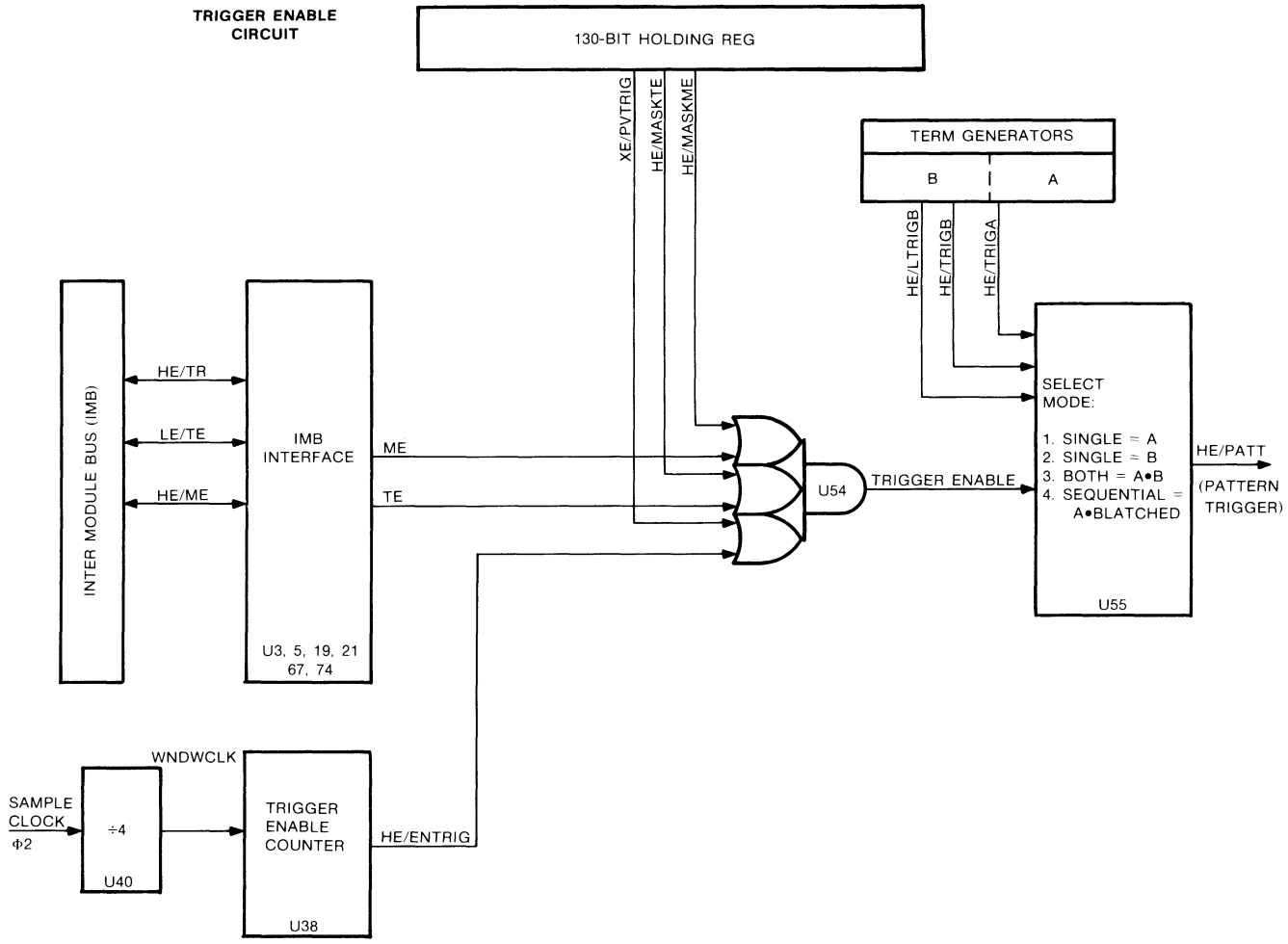


Figure 8-6.
Trigger Enable Circuit
Block Diagram

8-37. TRIGGER ENABLE CIRCUIT. (Figs. 8-5, 8-13)

8-38. The trigger enable circuit receives the qualified A, B, or B-Latched signals from the term generators. The trigger enable circuit can combine these signals into a pattern trigger, HE/PATT; or it can form a trigger from external commands via the IMB.

8-39. The glitch chip and the encoders on the acquisition board are between the probe and memory. Before a new run they contain old data from the last run. The trigger enable counter (U38) is programmed to hold off a trigger for several clocks, until the old data has been flushed from the system. The trigger enable counter also allows a certain amount of pre-trigger information to be viewed, even in start-trace modes. Since the trigger enable counter and the window counter (U36) are not fast enough to be clocked at the sample rate, they are clocked by the window clock (U40), which is one-fourth the rate.

8-40. The trigger enable circuit may drive, and be driven by, the IMB. The timing analyzer can enable, or be enabled by, other analyzers. The trigger (TR), trigger enable (TE), or master enable (ME) lines from the Inter Module Bus may all be used to enable the timing analyzer. The timing analyzer may also itself drive the TR, TE, and ME lines.

8-41. The trigger enable circuit also has a Post-Qualify Mode. When the HE/RESTARTEN (restart enable) line is high, the IMB TE line acts as a restart line, causing the timing analyzer to reset itself at the command of a second analyzer and look for another trigger. The TE line acts like a restart line in this mode; and the TR line acts like a hold line, preventing further resets.

8-42. The trigger enable circuit determines which term generator trigger, HE/TRIGA, HE/TRIGB, or HE/LTRIGB will become the pattern trigger HE/PATT that is sent on to the delay counter. The latched B trigger and the B trigger are mutually exclusive, but the A and B triggers may be anded.

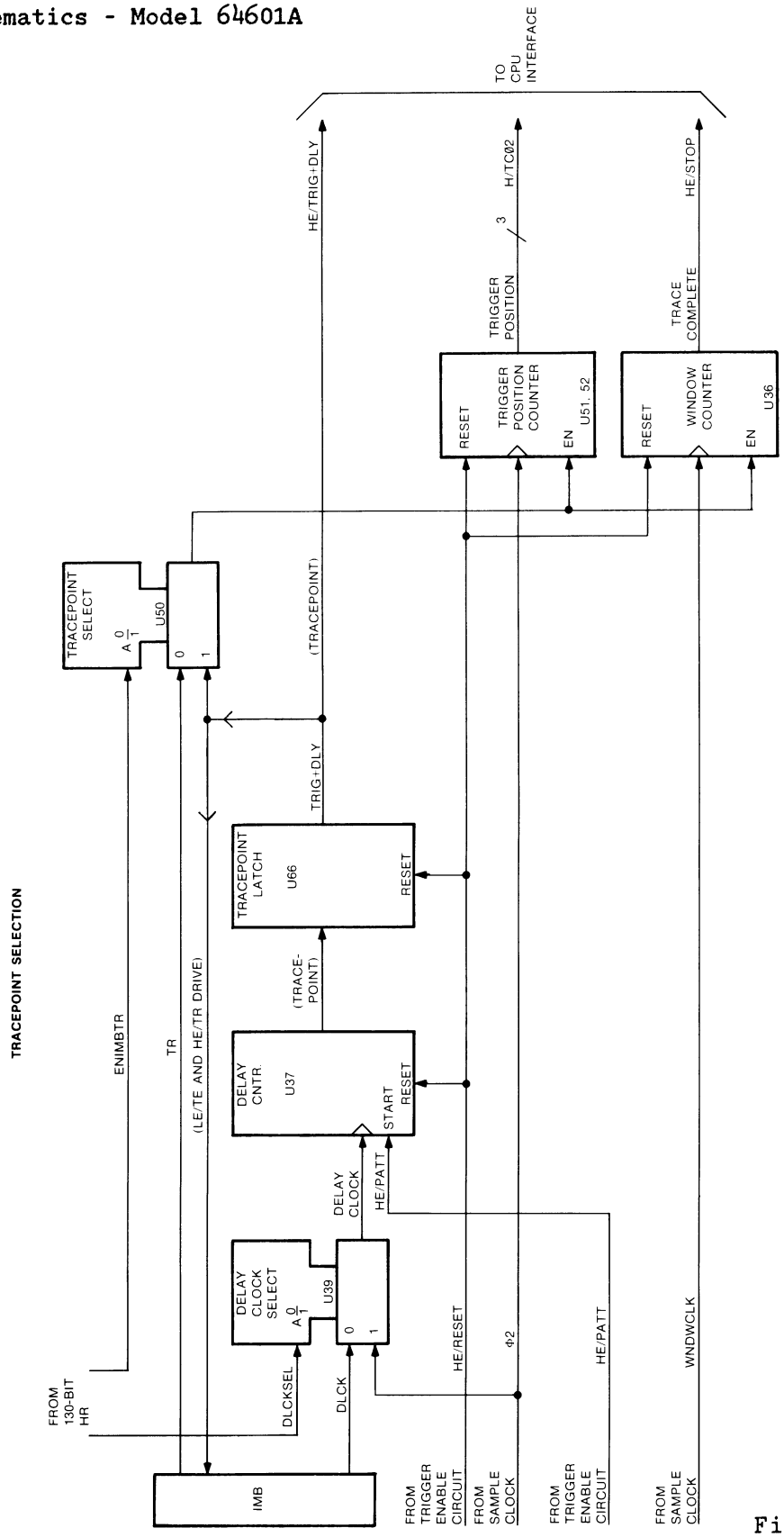


Figure 8-7.
Tracepoint Selection
Block Diagram

8-43. TRACEPOINT SELECTOR. (Figs. 8-6, 8-14)

8-44. "Tracepoint" is the start of a trace. The acquisition board provides a trigger signal to the control board when the pattern specification is satisfied. This trigger signal is further qualified in the control board: (1) It can be ANDed or ORed with a trigger from a second aquisition board. (2) It can be armed by signals from the IMB. (3) It can be delayed. (4) It can be qualified as to pattern duration and transition. The final qualified trigger (HE/TRIG+DLY) that starts a trace is called tracepoint.

8-45. The tracepoint selector receives the qualified pattern trigger, HE/PATT, from the Trigger Enable Circuit. The tracepoint selector can add delay to the timing trigger; or it can ignore the timing trigger entirely, and trigger the analyzer via the IMB.

8-46. The tracepoint selector is also programmed by the 130-bit holding register to determine the amount of "window" between tracepoint in memory and the end of new acquisition. That is, the tracepoint selector generates HE/STOP, which stops the sample clock, ending the trace.

8-47. The tracepoint selector allows the mainframe to determine the exact position of tracepoint in memory. This is necessary because the acquisition RAM is loaded from eight-bit serial-to-parallel shift registers. Thus the memory write pulses and the memory address counter clocks occur at one-eighth sample frequency. Without additional circuitry in the tracepoint selector, the position of the trigger in memory could be known only to an eight-bit-group accuracy.

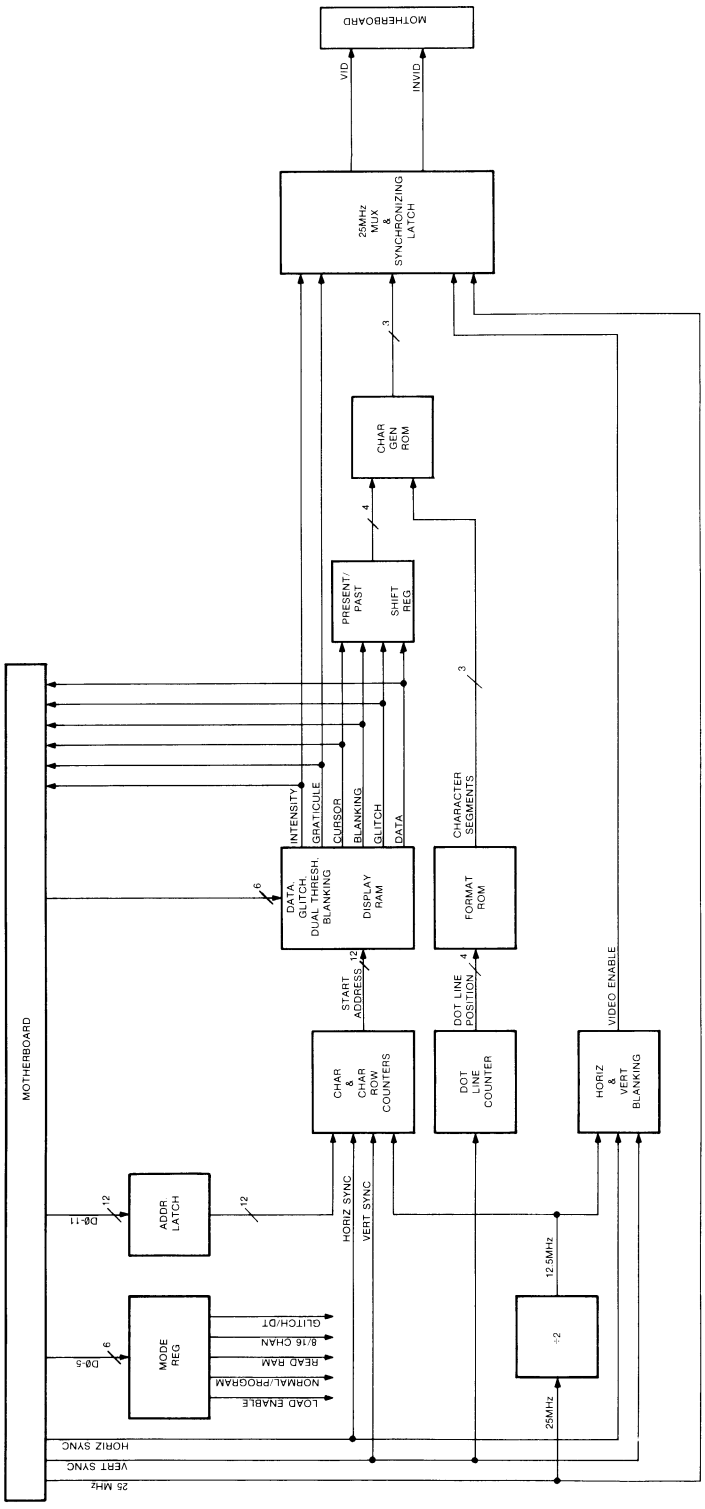


Figure 8-8.
Display Driver
Block Diagram

8-48. DISPLAY DRIVER. (Figs. 8-7, 8-15, 8-16)

8-49. The timing analyzer has its own display driver, which provides the timing characters, enhancements, and blanking to the mainframe for display. The mainframe receives the display driver video, programs the display to start at a particular portion of the screen, supplies horizontal and vertical synchronizing pulses, and selects the order and number of the probe channels displayed.

8-50. The display driver produces a 512-by-240 dot display. Each character is two dots wide; in the 8-channel mode a character is 30 dots high, and in the 16-channel mode 15 dots high.

8-51. The display driver has two modes of operation. In the programming mode the mainframe presets the character counter, the character-row counter, and the dot-line counter with starting addresses for the display. The mainframe also loads the display RAMs with data, glitch, blanking, cursor, intensify, and graticule information. In the normal mode, the timing analyzer actually sends video and inverse video to the mainframe for display.

8-52. The character counters are capable of counting 255 2-dot characters, but are preset to less to allow for a left margin. The dot-line counters count the number of horizontal dot-lines in the display. Since only one line of a character is written at a time, the dot-line counter increments each time horizontal sync (L/HSYN) pulses. The character-row counter counts the number of character rows (eight in 8-channel mode) and increments every 30 lines in 8-channel mode, or every 15 lines in 16-channel mode.

8-53. The mainframe loads the encoded timing information into the display RAMs during the programming mode. Since transitions require knowledge of past data, RAM information is sent to a "present/past" shift register, which delays data by one dot during display. Both old and new data are then sent to a character ROM, which also receives information from the formatting ROM. Since only one line of a character is written at a time, and characters such as dualthresholds have "middle" information, horizontal trace position is needed to format characters. The formatting ROM, after getting the horizontal position from the dot-line counter, outputs a 3-segment code which correlates horizontal position with character type.

8-54. The character ROM encodes data and formatting information into two dots of video. The mainframe writes dots on the screen at a 25MHz rate; but since each character is two dots wide, 12.5MHz has been used up to this point in the display driver. The two 12.5MHz parallel dots are therefore changed to serial information and synchronized with the 25MHz system clock in the output latch.

8-55. Since data, enhancements, and blanking have taken different paths, they need to be synchronized. The output latch "lines up" the information so that the data may be enhanced and blanked; and the resulting video is sent out to the mainframe.

8-56. MNEMONICS.

8-57. Mnemomics are listed in alphabetical order following the slash. The following convention is used:

a. An L or H before the slash indicates active LOW or HIGH.

b. An E after L or H, but before the slash, indicates an ECL signal.

c. No E before the slash indicates a TTL signal.

d. An X instead of L or H means the signal may be programmed as either active LOW or HIGH.

e. The functional mnemonic appears after the slash.

Table 8-1. Mnemonics

MNEMONIC	DEFINITION
HE/AND	Determines AND/OR combination of XE/TRIG signals from two acquisition boards.
HE/ATRANSIT	A transition. Enables an A trigger on the transition "leaving" the specified pattern. To trigger on "entering" transitions, XE/TRIG from the acquisition board must be LOW true.
HE/BLATCHR	B latch reset. Resets B latch for B-Latched mode.
L/BLNKMEM	Enable display blanking memory.
HE/BTRANSIT	B transition. Enables a B trigger on the transition "leaving" the specified pattern. To trigger on "entering" transitions, XE/TRIG from the acquisition board must be LOW true.
H/CHARAD0-11	Character address. Addresses to display RAM from the character and line counters.

MNEMONIC	DEFINITION
L/CNTRLD	Counter load. Clocks character, dot-line, and character-row counters in the display circuits during the programming mode. During normal counting, 12.5MHz clocks these counters. Derived from L/MEMWRT.
HE/DLCLK	Delay clock. The timing analyzer delay counter (U37) may be clocked externally over this IMB line.
L/DATAMEM	Enable display data memory.
HE/DLYCLKSEL	Delay clock select. Selects a clock for the delay counter (U37), which may be clocked internally or via the IMB.
L/D0-15	Data lines from motherboard.
HE/D15	Derived from data line 15. Programs the 130-bit register.
L/ENHANMEM	Enable display enhancement memory.
LE/ENDRIVME	Enables the timing analyzer to drive the IMB LE/ME (master enable) line true when a valid trigger occurs.
LE/ENDRIVTE	Enables the timing analyzer to drive the IMB LE/TE (trigger enable) line true when a valid trigger occurs.
LE/ENDRIVTR	Enables the timing analyzer to drive the IMB LE/TR (trigger) line true when a valid trigger occurs.
LE/ENIMBTR	Enable IMB trigger. Enables the IMB TR line to determine trace-point externally.
LE/ENLATCHB	Enables a latched B trigger. Causes a trigger if A occurs anytime following B.
LE/ENPVTRIG	Enables a performance verification trigger.
LE/ENTRIGA	Enables a trigger out of the A term generator.
LE/ENTRIGB	Enables a trigger out of the B term generator.
LE/ENTRIG1A	Enables a trigger into the A term generator from the acquisition board in the lower numbered slot.

MNEMONIC	DEFINITION
LE/ENTRIG2A	Enables a trigger into the A term generator from a second acquisiton board in the higher numbered slot.
LE/ENTRIG3A	Enables a trigger into the A term generator from a third acquisition board. Not used in a 200MHz system.
LE/ENTRIG4A	Enables a trigger into the A term generator from a fourth acquisition board. Not used in a 200MHz system.
LE/ENTRIG1B	Enables a trigger into the B term generator from the acquisition board in the lower numbered mainframe slot.
LE/ENTRIG2B	Enables a trigger into the B term generator from a second acquisition board in the higher numbered mainframe slot.
LE/ENTRIG3B	Enables a trigger into the B term generator from a third aquisition board. Not used on the 200MHz system.
LE/ENTRIG4B	Enables a trigger into the B term generator from a fourth acquisition board. Not used on the 200MHz system.
HE/F1 * HE/F2 * HE/F3 * HE/F4 *	Selects the sample clock frequency.
L/GLTCHMEM	Enable display glitch memory.
HE/HRCLK	Holding register clock. Clocks programming into the 130-bit control register.
L/HSYN	Horizontal synchronizing signal for display from the mainframe.
L/IVID	Inverse video to motherboard.
L/LOADEN	Load enable. Enables presetting the display counters with an address for the display RAMs during the programming mode.
L/LOADUR	Load duration. Clocks in pattern duration specification.
HE/LTRIGB	Latched B trigger signal. HE/TRIGB must be false. A trigger will occur when A occurs anytime after B.
HE/MASKME	Mask master enable. Masks the IMB master enable signal. Must be low if ME from the IMB is to enable the trigger.

MNEMONIC	DEFINITION
HE/MASKTE	Mask trigger enable. Masks the IMB trigger enable signal. Must be low if TE from the IMB is to enable the trigger.
H/MEMFUL	Memory full. Indicates when memory has been completely filled with good data at least once. Status bit to processor.
L/MEMWRT	Enables write to display memory.
L/MODEN	Mode enable. Enables display mode register.
HE/PATT	Pattern trigger. Internal trigger signal after being qualified by term generators, but before delay is inserted. External trigger may also be asserted at this point.
H/PATTOUT(BNC4)	Pattern trigger output to the BNC4 jack on the mainframe.
LE/PDUR>A	Pattern duration greater than A specifies. Enables triggering on patterns with durations greater than specified by the A term generator. High for "less than" durations.
LE/PDUR>B	Pattern duration greater than B specifies. Enables detection of patterns with durations greater than specified by the B term generator. False, or high, for "less-than" widths.
HE/phi2C1	Derived from phi2 sample clock. Used to clock the delay counter if HE/DLCLK (delay) from the IMB is not selected.
HE/phi2C2	Derived from phi2 sample clock. Clocks the position counter, which determines exact trigger position in an eight-bit sample group. Also used to derive H/WNDWCLK for the window and trigger enable counters.
HE/phi2,	Sample clock from sample rate generator to the acquisition boards.
L/PROGRAM	Selects programming mode for timing display. This mode is used for loading the display RAMs. When high, the display, or normal, mode is selected.
LE/PVCLK	Performance verification sample clock from the mainframe.
HE/PVSTOP	Stops the sample clock during performance verification.

MNEMONIC	DEFINITION
XE/PVTRIG	Used instead of a acquisition-board trigger during performance verifcation. Can be either HIGH or LOW, depending on whether ANDing or ORing triggers.
L/POP	Power-on-pulse from motherboard.
HE/PROCRESET	Processor reset. Used by the mainframe to drive HE/RESET.
H/RCNTR0-3	Row counter output. Addresses to the Character-Row RAM.
HE/RESET	Master reset or initialization.
HE/RESTARTEN	Enables a restart on receipt of a high-going LE/TE transition from the IMB. Sets the Post-Qualify mode, which allows LE/TE to act like a restart signal.
LE/RUN	Enables run mode. When high, stops the sample clock.
HE/RUN	Enables run mode on the acquisition board via the timing bus.
H/SCLKOUT(BNC3)	Sample clock output before the last divider. Output to a BNC connector.
L/STARTADR	Start address. Clocks in the starting address for the display.
HE/STOP	Stops acquisition. Window counter (U36) output, which determines the position of the trigger in memory (ie, the window in memory between tracepoint and the end-of-acquisition).
H/TC0,H/TC1, H/TC2	Trigger position count. Determine the exact trigger position within an eight-sample clock group. Status bits to mainframe.
LE/TEARM	Trigger enable arm. Will arm the trigger when L/TE from the IMB is true.
LE/TEDRIVE	Trigger enable drive. Signal used by the timing analyzer to drive the IMB LE/TE (trigger enable) line.
HE/TR	Trigger. The timing analyser can be triggered, or can assert a trigger on this IMB line.
HE/TRDRIVE	Trigger drive. Signal used by the timing analyzer to drive the IMB HE/TR (trigger) line.

MNEMONIC	DEFINITION
LE/TRDRVTE	Trigger drives trigger enable. The received HE/TR from the IMB is used to drive the IMB LE/TE line.
HE/TRIGTEST	Enables trigger for performance verification.
HE/TRIGA	Trigger signal qualified by the A term generator.
HE/TRIGB	Trigger signal qualified by the B term generator.
H/TRIG+DLY	Trigger plus delay. Tracepoint--the position of the trigger in in memory, plus any delay added by the timing analyzer's delay counter or by another analyzer via the IMB.
L/VID	Video from display driver to motherboard.
L/VSYN	Vertical synchronizing signal for display from the mainframe.
HE/WNDWCLK	Window clock. Clock to window (U36) and trigger enable (U38) counters.
H/12.5MHz, L/12.5MHz	Derived from the 25MHz. mainframe system clock. Used as the timing display character clock, since each timing character is two dots wide.
25MHz CLK	Mainframe system clock. Used by the timing display as the dot frequency.

NOTES

ETCHED CIRCUIT BOARD

FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

SCREWDRIVER ADJUSTMENT

TP1 ELECTRICAL TEST POINT TP (WITH NUMBER)

NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.

LETTERED TEST POINT NO MEASUREMENT AID PROVIDED

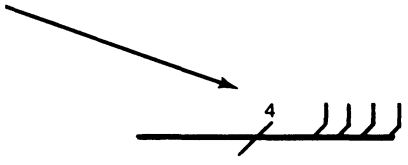
COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.

1 3 NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION. LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

A CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS



(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

STD-20-09-81

Table 8-2. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

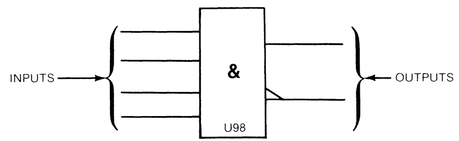
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

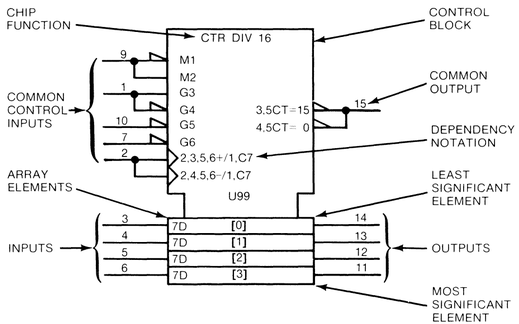
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

LS-08-09-82 - 1

Table 8-2. Logic Symbols (Cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

LS-08-09-82 - 2

Table 8-2. Logic Symbols (Cont'd)

OTHER SYMBOLS

- Analog Signal
- & AND
- Bit Grouping
- Buffer
- ! Compare
- Dynamic
- =1 Exclusive OR
- Hysteresis
- ? Interrogation
- Internal Connection
- Inversion
- O Negation
- Nonlogic Input/Output
- Open Circuit (external resistor)
- Open Circuit (external resistor)
- ≥1 OR
- Passive Pull Down (internal resistor)
- Passive Pull Up (internal resistor)
- Postponed
- ← Shift Left (or up)
- → Shift Right (or down)
- / Solidus (allows an input or output to have more than one function)
- ▽ Tri-State
- , Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
- ( ) Used for factoring terms using algebraic techniques.
- [ ] Information not defined.
- Φ Logic symbol not defined due to complexity.

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	-	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

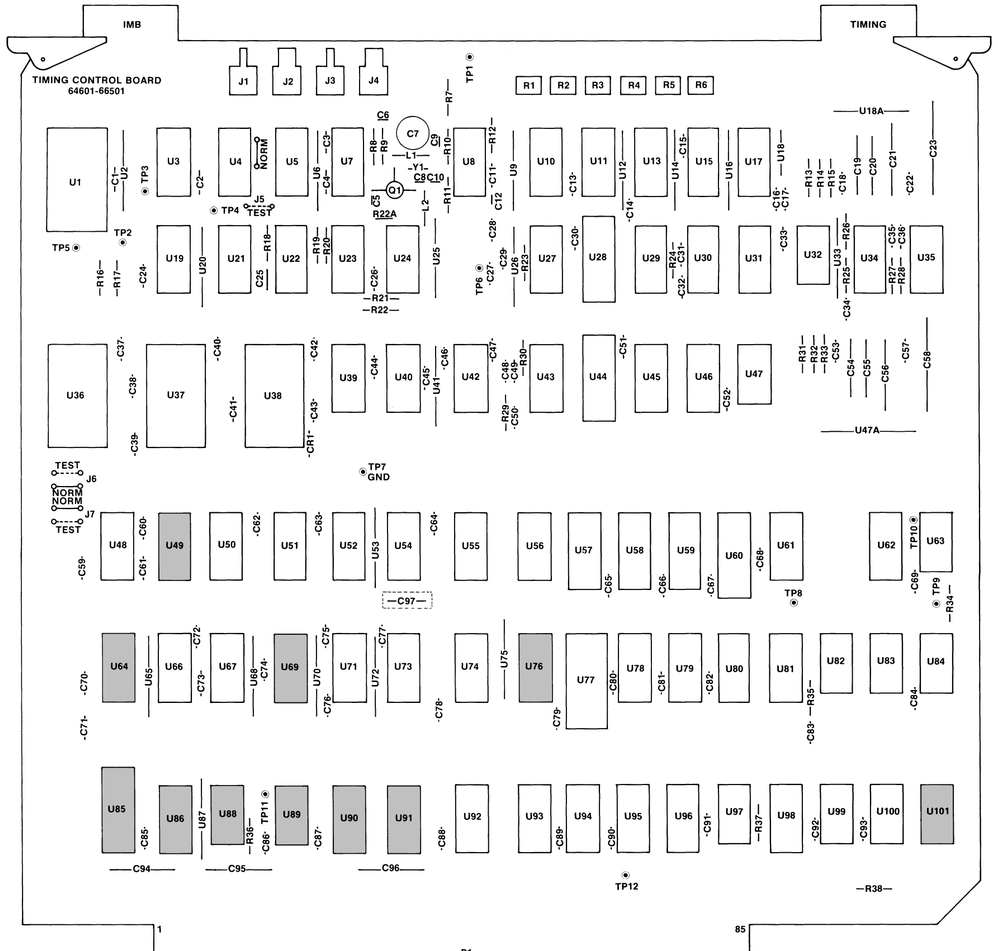
CHIP FUNCTIONS

BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

- Astable
- 100 ns Delay
- Nonretriggerable Monostable
- NV Nonvolatile
- Retriggerable Monostable

LS-08-09-82 - 3


IMB
TIMING
TIMING CONTROL BOARD
64601-66501
J1
J2
J3
J4
TP1
R1
R2
R3
R4
R5
R6
U1
U2
U3
U4
NORM
U5
U6
U7
C6
C7
C8
C9
C10
L1
L2
Y1
Q1
R22A
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U18A
C23
TP3
TP4
J5
TEST
TP2
TP5
U19
U20
U21
U22
U23
U24
U25
R21
R22
TP6
TP7
GND
U26
U27
U28
U29
U30
U31
U32
U33
U34
U35
U36
U37
U38
U39
U40
U41
U42
U43
U44
U45
U46
U47
U47A
CR1
J6
J7
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U49
U50
U51
U52
U53
U54
U55
U56
U57
U58
U59
U60
U61
U62
TP10
U63
C97
TP8
TP9
R34
U64
U65
U66
U67
U68
U69
U70
U71
U72
U73
U74
U75
U76
U77
U78
U79
U80
U81
U82
U83
U84
U85
U86
U87
U88
TP11
U89
U90
U91
U92
U93
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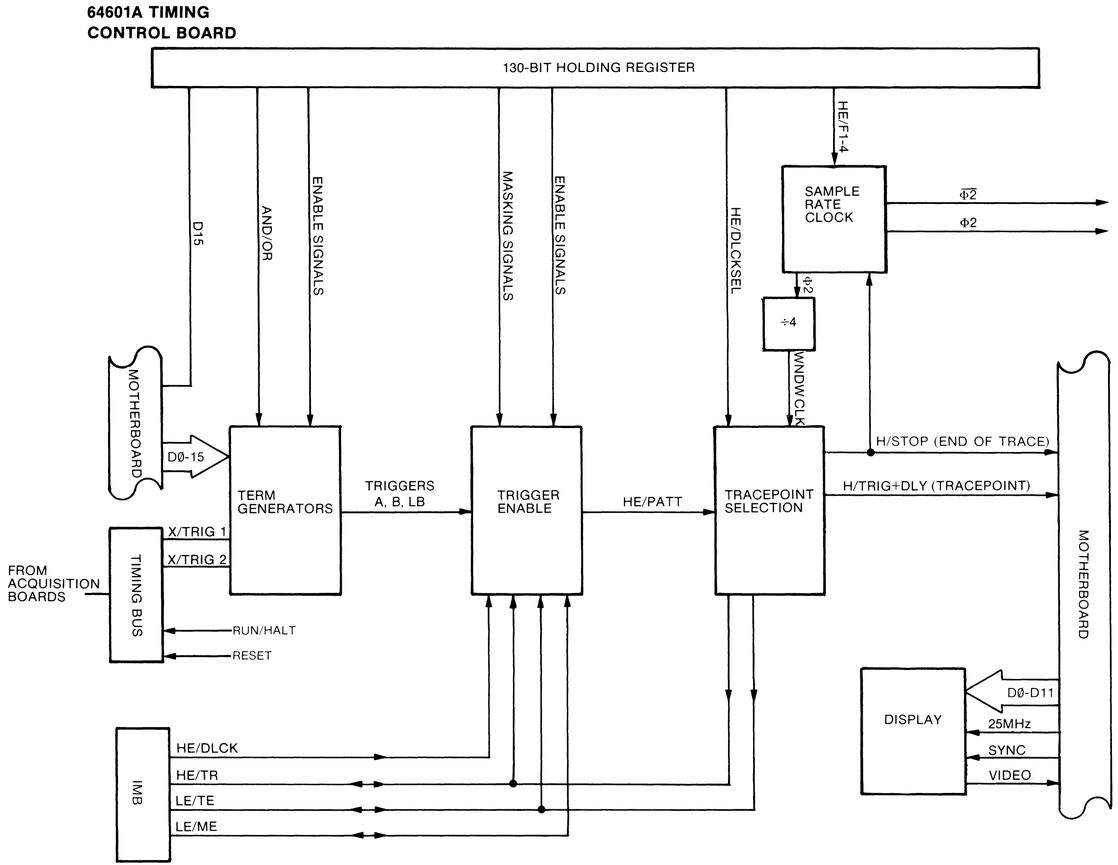
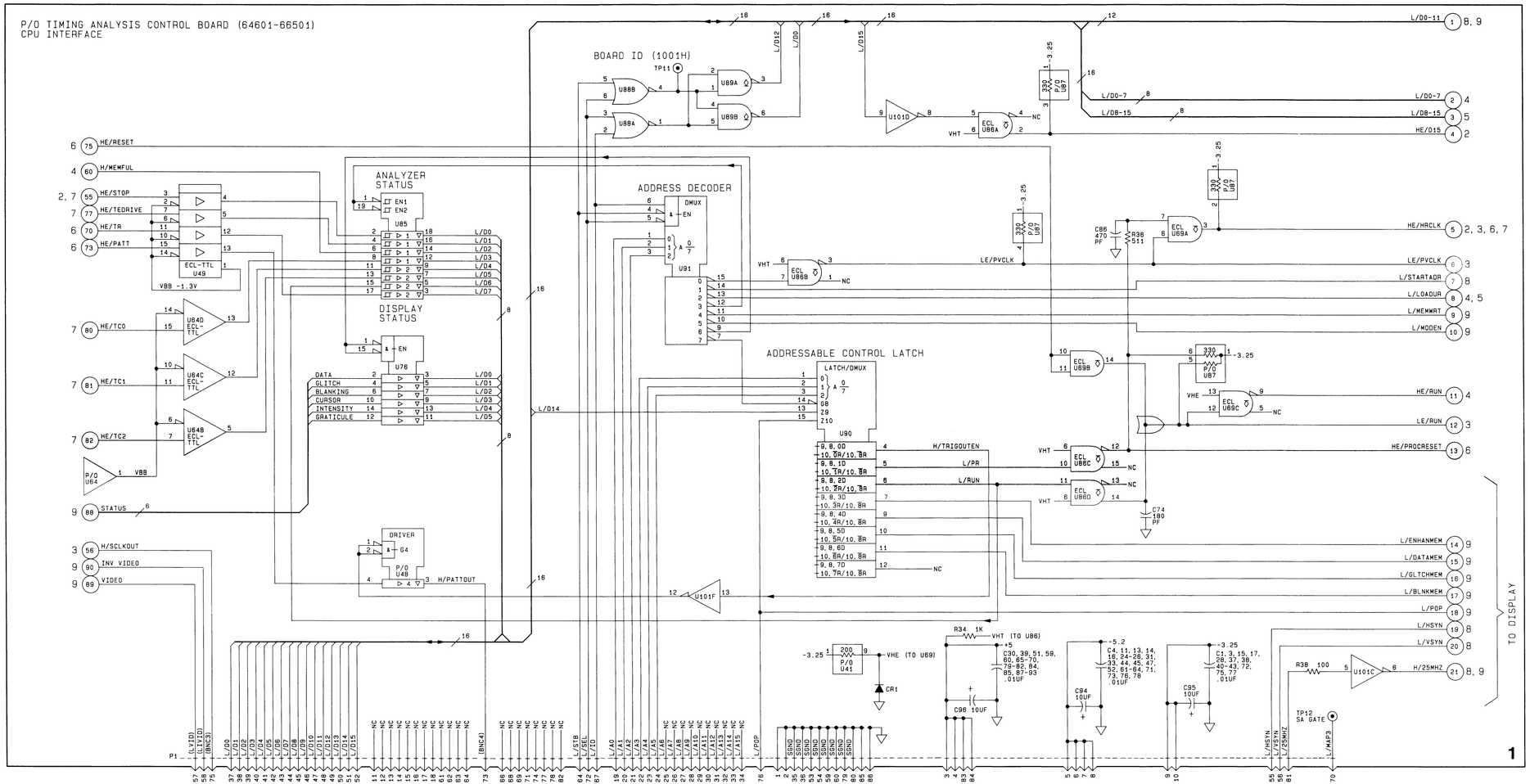
U99
U100
U101
C94
C95
C96
TP12
R38
1
85
P1


64601A TIMING
CONTROL BOARD
130-BIT HOLDING REGISTER
HE/F1-4
D15
AND/OR
ENABLE SIGNALS
MASKING SIGNALS
ENABLE SIGNALS
HE/DLCKSEL
SAMPLE
RATE
CLOCK
Φ2
Φ2
÷4
WNDW CLK
MOTHERBOARD
DØ-15
TERM
GENERATORS
TRIGGERS
A, B, LB
TRIGGER
ENABLE
HE/PATT
TRACEPOINT
SELECTION
H/STOP (END OF TRACE)
H/TRIG+DLY (TRACEPOINT)
MOTHERBOARD
FROM
ACQUISITION
BOARDS
TIMING BUS
X/TRIG 1
X/TRIG 2
RUN/HALT
RESET
DISPLAY
DØ-D11
25MHz
SYNC
VIDEO
IMB
HE/DLCK
HE/TR
LE/TE
LE/ME



ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr. Part No.
U49,64	1820-1052	MC10125L
U69	1820-1400	MC10104P
U76	1820-1641	SN74LS365AN
U85	1820-1917	74LS240N
U86	1820-1173	MC10124L
U88	1820-1322	SN74S02N
U89	1820-0269	SN7403N
U90	1820-2799	SN74LS259
U91	1820-1216	SN74LS138N
U101	1820-0683	SN74S04N

PARTS ON THIS SCHEMATIC

C1,3,4,11,13-17,24-26,28,30,31,33,
37-45,47,51,52,59-82,84-96
CR1
R34,36,38
U87 (RESISTOR PACK)

IC POWER SUPPLY CONFIGURATION

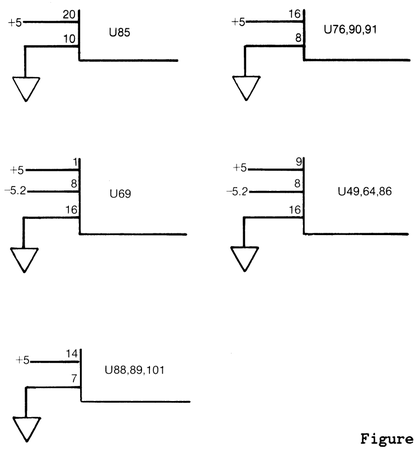
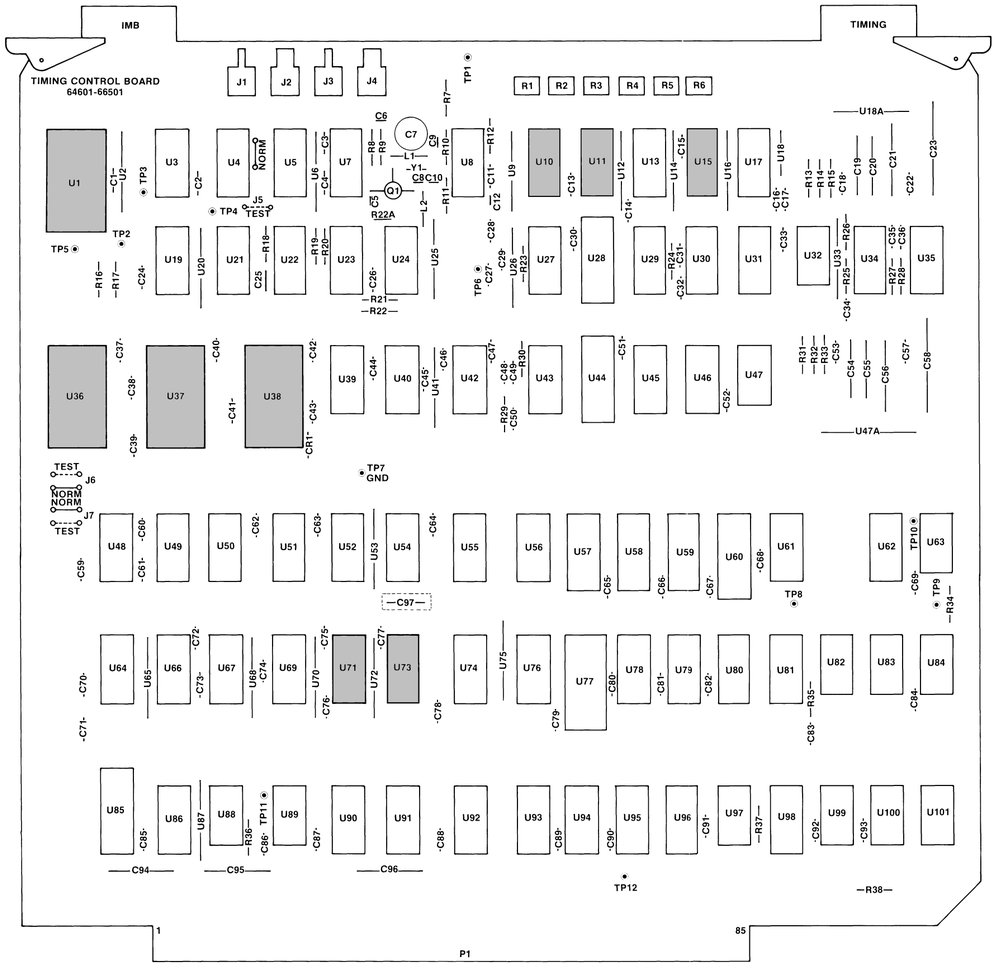
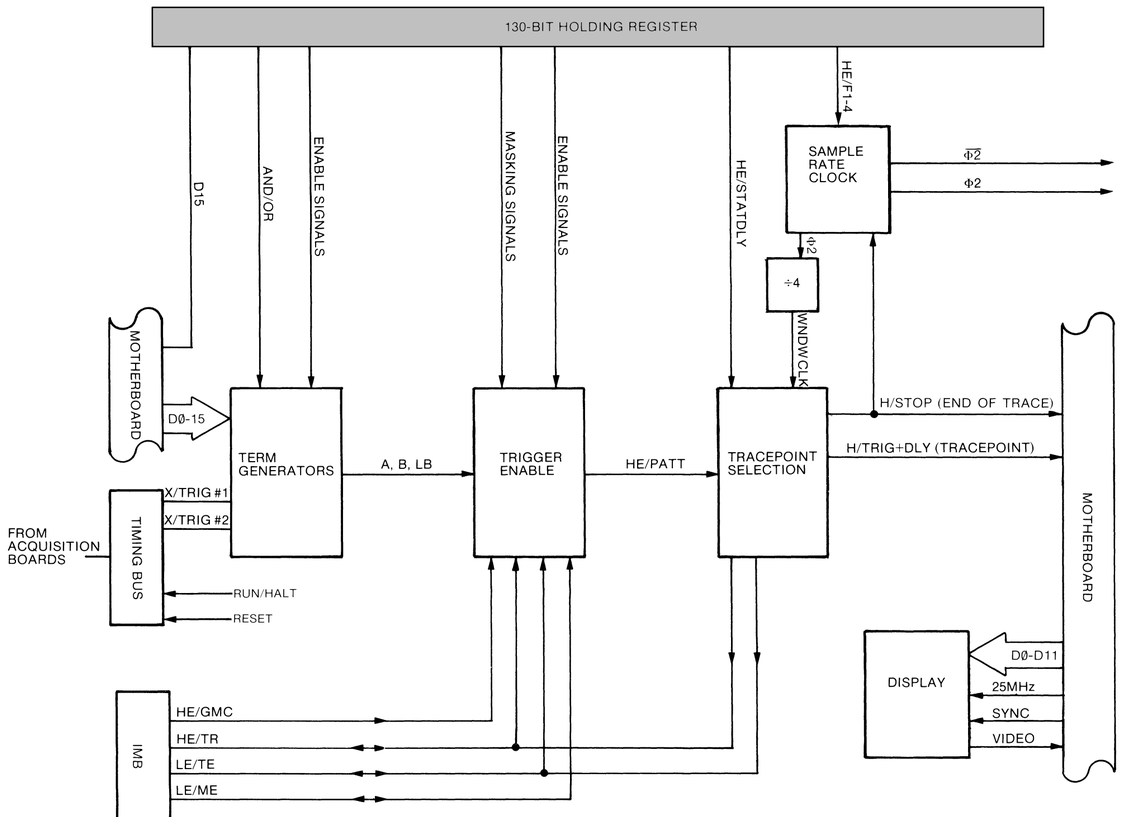
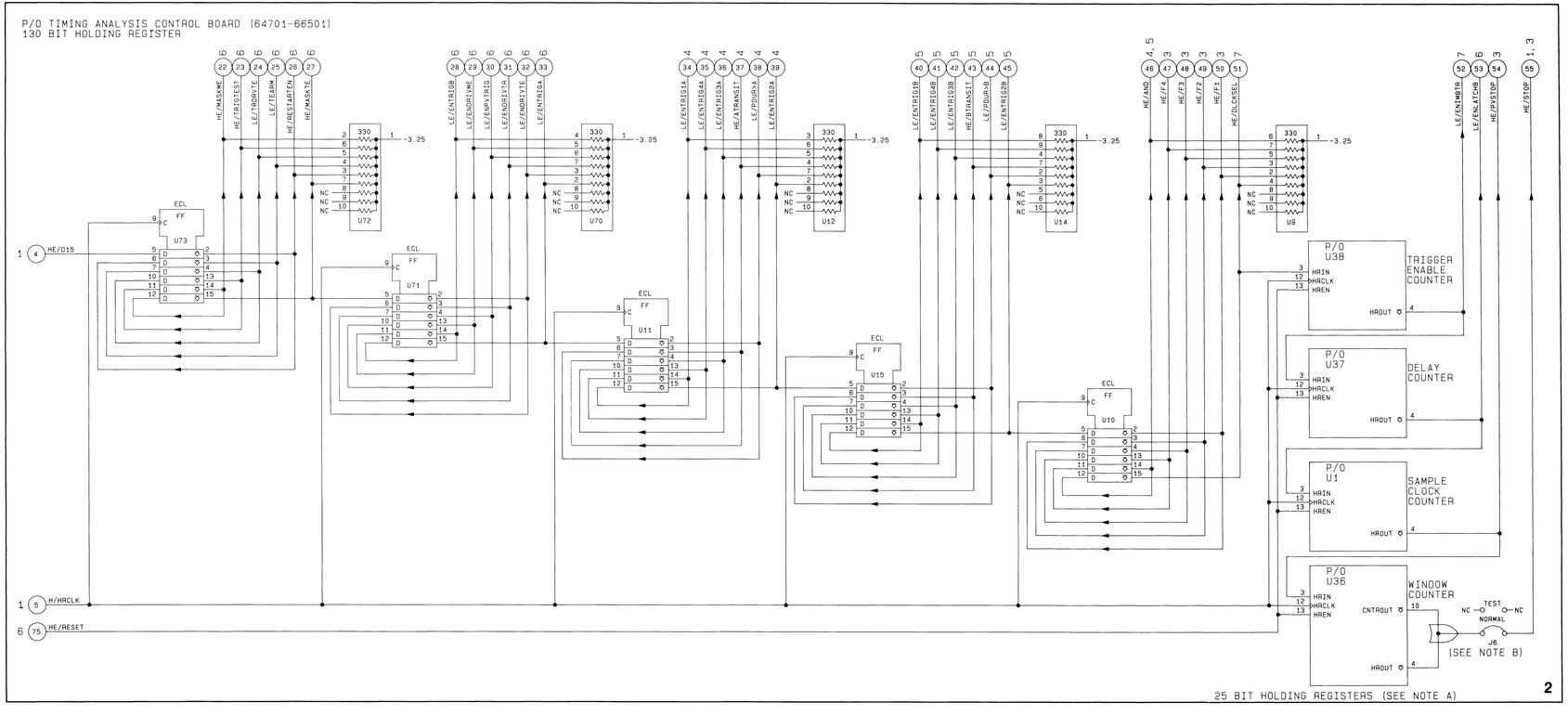


Figure 8-9.
Service Sheet 1
CPU Interface
CTL 8-25



64601A TIMING CONTROL BOARD





ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr. Part No.
U10,11,15 71,73	1820-2193	MC10176L
U1,36,37,38	1NB4-5008	1NB4-5008

PARTS ON THIS SCHEMATIC

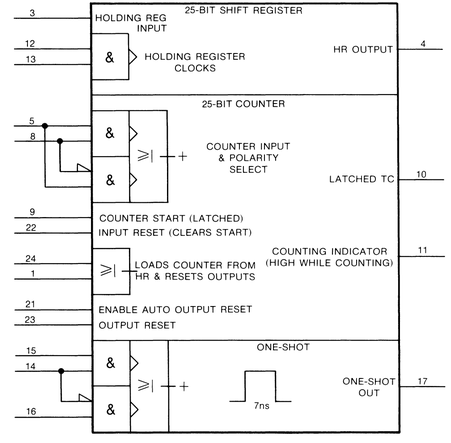
U9,12,14,70,72 (RESISTOR PACKS)

NOTE A:

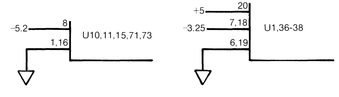
Only the holding register part of U1, 36,37,38 is shown on this schematic. For the remainder, see the following service sheets:

U1----------3 U38---------6
U36-37-------7

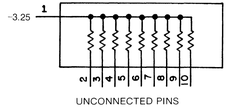
U1, 36,37,38



IC POWER SUPPLY CONFIGURATION



RESISTOR PAKS U9,12,14,70,72

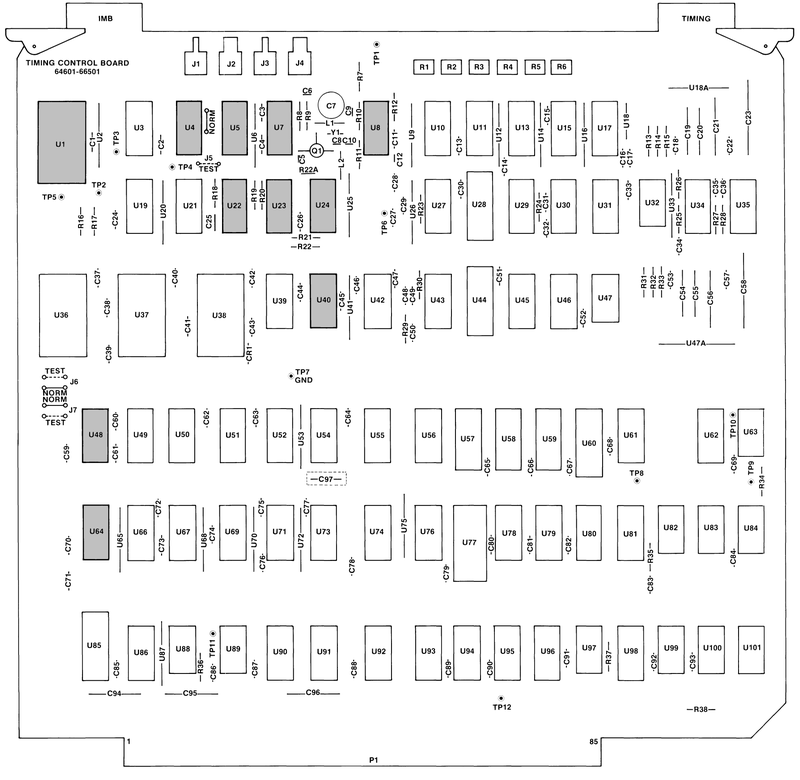


UNCONNECTED PINS
U9 - PINS 8,9,10
U12 - PINS 8,9,10
U14 - PINS 5,6,10
U70 - PINS 8,9,10
U72 - PINS 8, 10

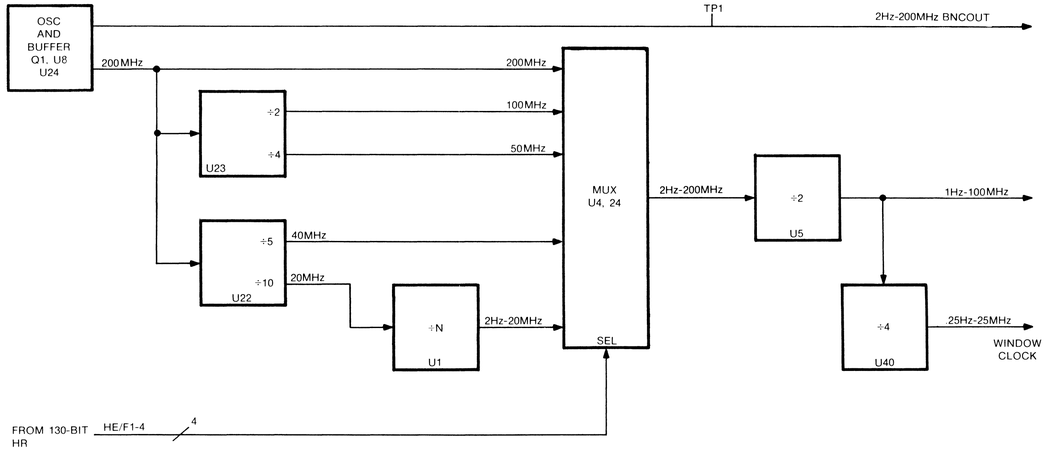
NOTE B:

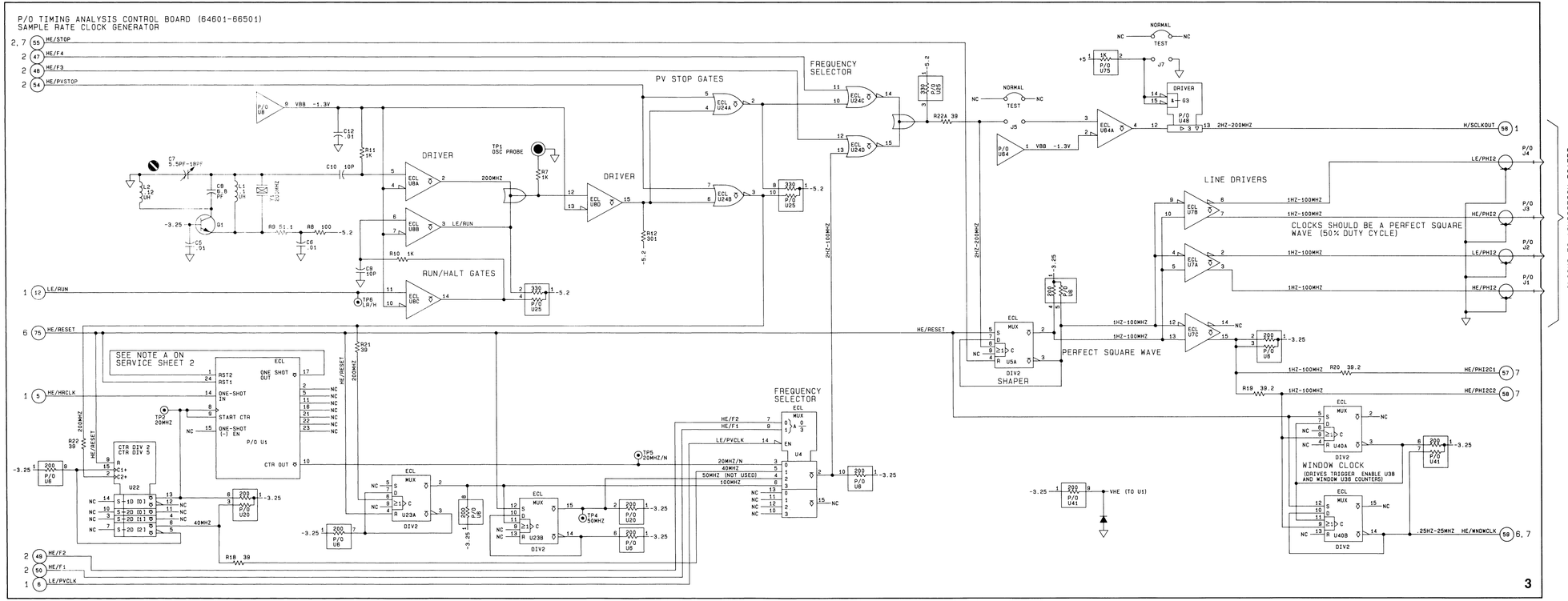
J6 is duplicated on both service sheet 2 and 7.

Figure 8-10.
Service Sheet 2
130-Bit Control Shift Register
CTL 8-27



SAMPLE CLOCK





ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr. Part No.
U1	1NB4-5008	
U4	1820-1359	MC10174P
U5,23	1820-1225	MC10231P
U7	1820-1320	MC10216L
U8	1820-0920	MC1692L
U22	1820-2664	MC1678L
U24	1820-0796	MC1662L
U40	1820-1225	MC10231P
U48	1820-0780	DS8831N
U64	1820-1052	MC10125L

PARTS ON THIS SCHEMATIC

TP1,2,4-6
J5,7
Q1
Y1
L1,2
C5-9,12
R1,8-12,18-20,22
U6,20,25,41,75 (RESISTOR PACKS)

IC POWER SUPPLY CONFIGURATION

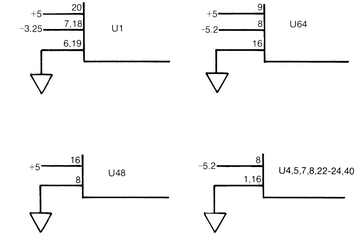
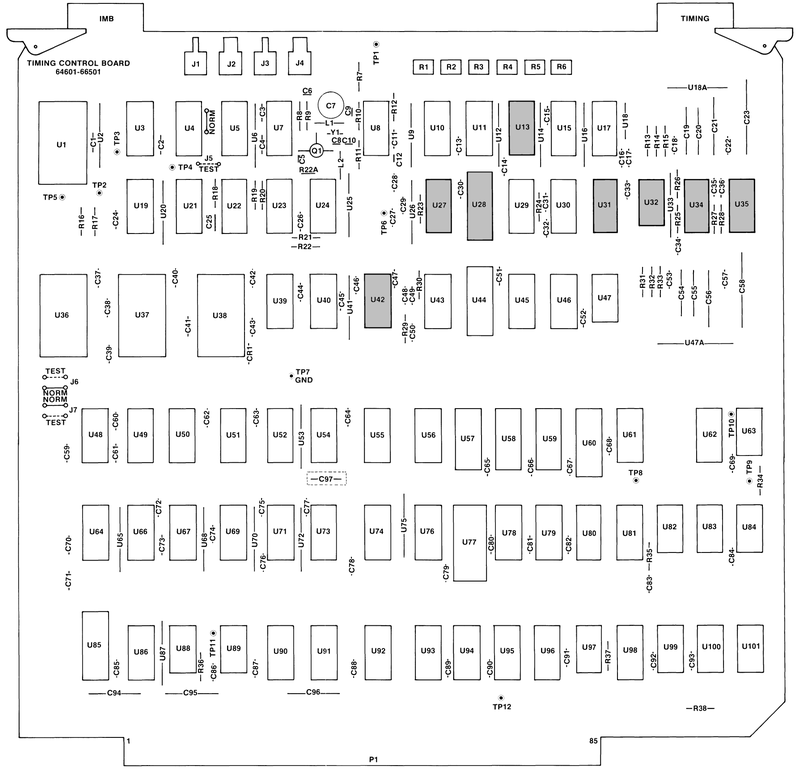
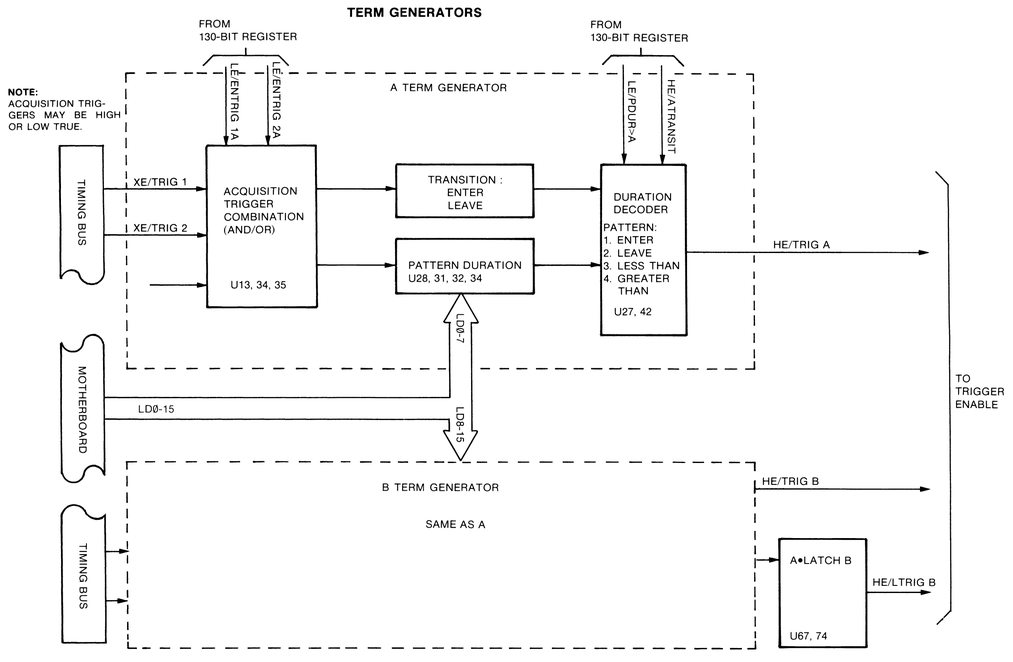


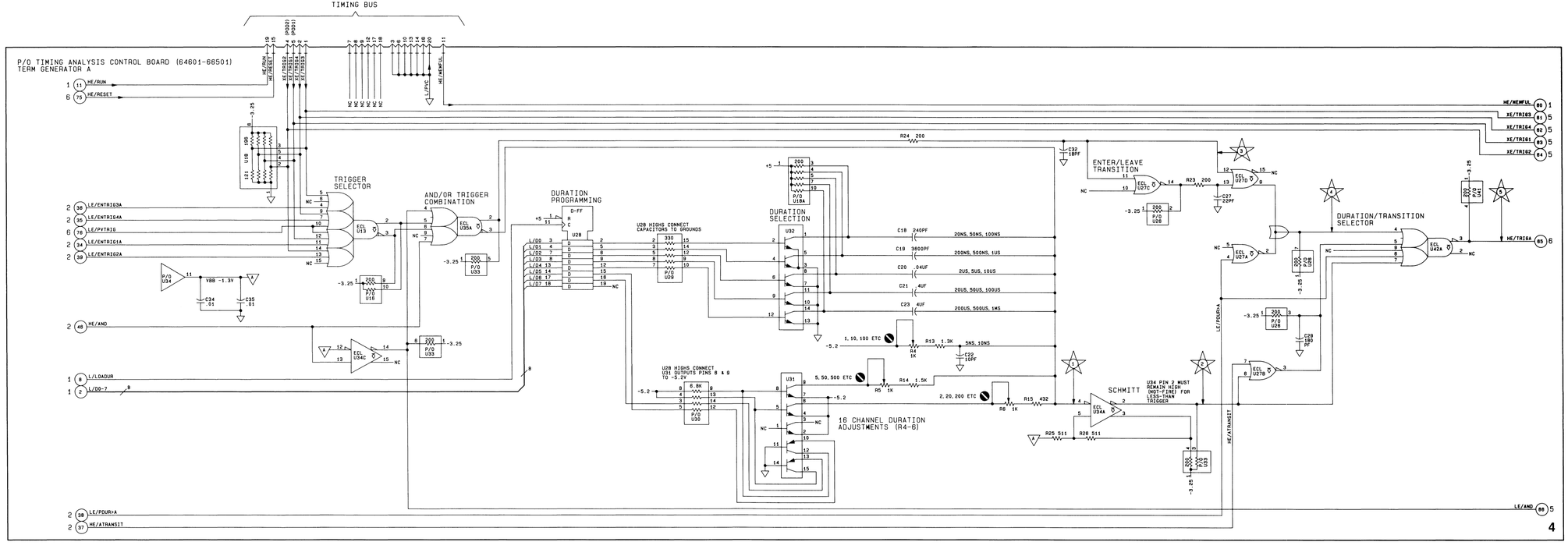
Figure 8-11.
Service Sheet 3
Sample Clock
CTL 8-29





WAVEFORM	IC PIN	ENTERING	LEAVING	LESS THAN
1	U34-4			
2	U34-2			
3	U27-11,12			
4	U27-9			
5	U42-3			

XE/TRIG	HE/TRANSIT	LE/PDUR>	PATTERN MUST BE:
H	X	L	GREATER THAN SPECIFIED
H	L	H	LESS THAN SPECIFIED
H	H	H	TRANSITION LEAVING
L	H	H	TRANSITION ENTERING



ICs ON THIS SCHEMATICS

Ref Des	HP Part No.	Mfr. Part No
U13	1820-0815	MC10121P
U27	1820-0802	MC10102P
U28	1820-1730	SN74LS273N
U31	1858-0054	
U32	1821-0002	CA3054
U34	1820-1320	MC10216L
U35,42	1820-1946	MC10117L

PARTS ON THIS SCHEMATIC

C18-23,27,29,32,34,35
R4-6,13-15,23-26
U16,18,18A,26,29,30,33,41 (RESISTOR PACKS)

IC POWER SUPPLY CONFIGURATION

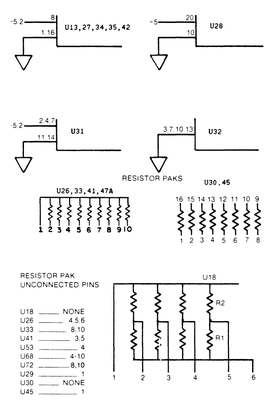
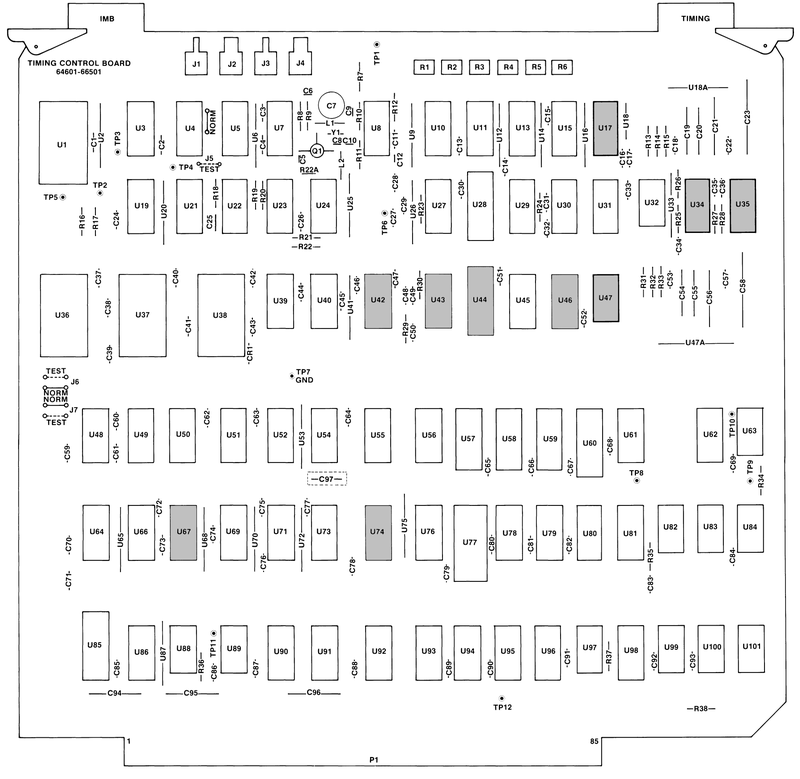
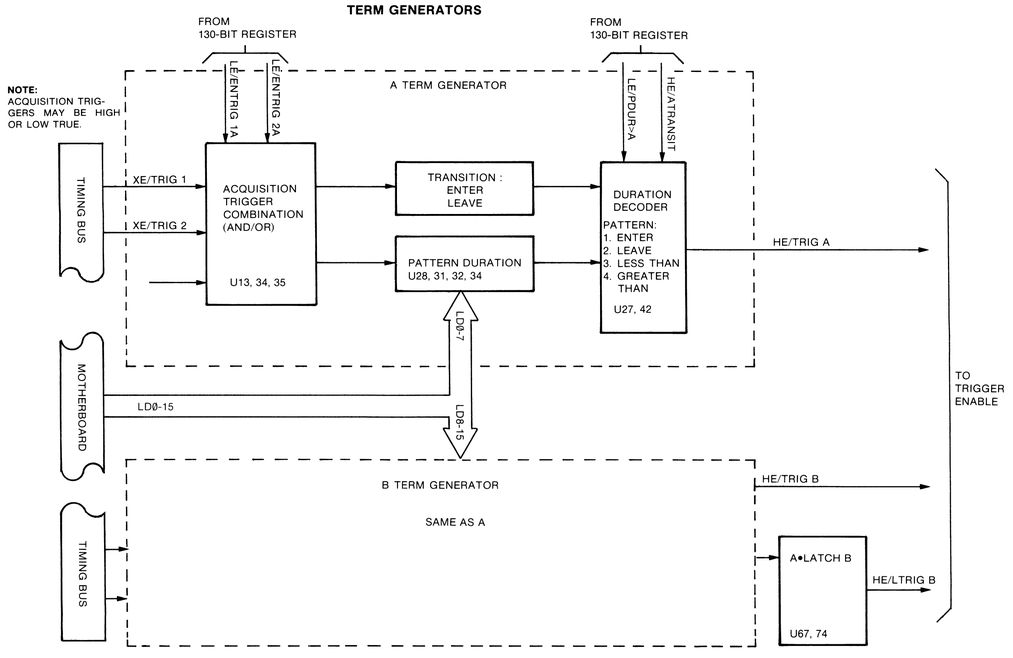


Figure 8-12.
Service Sheet 4
Term Generator A
CTL 8-31
CHANGE 1

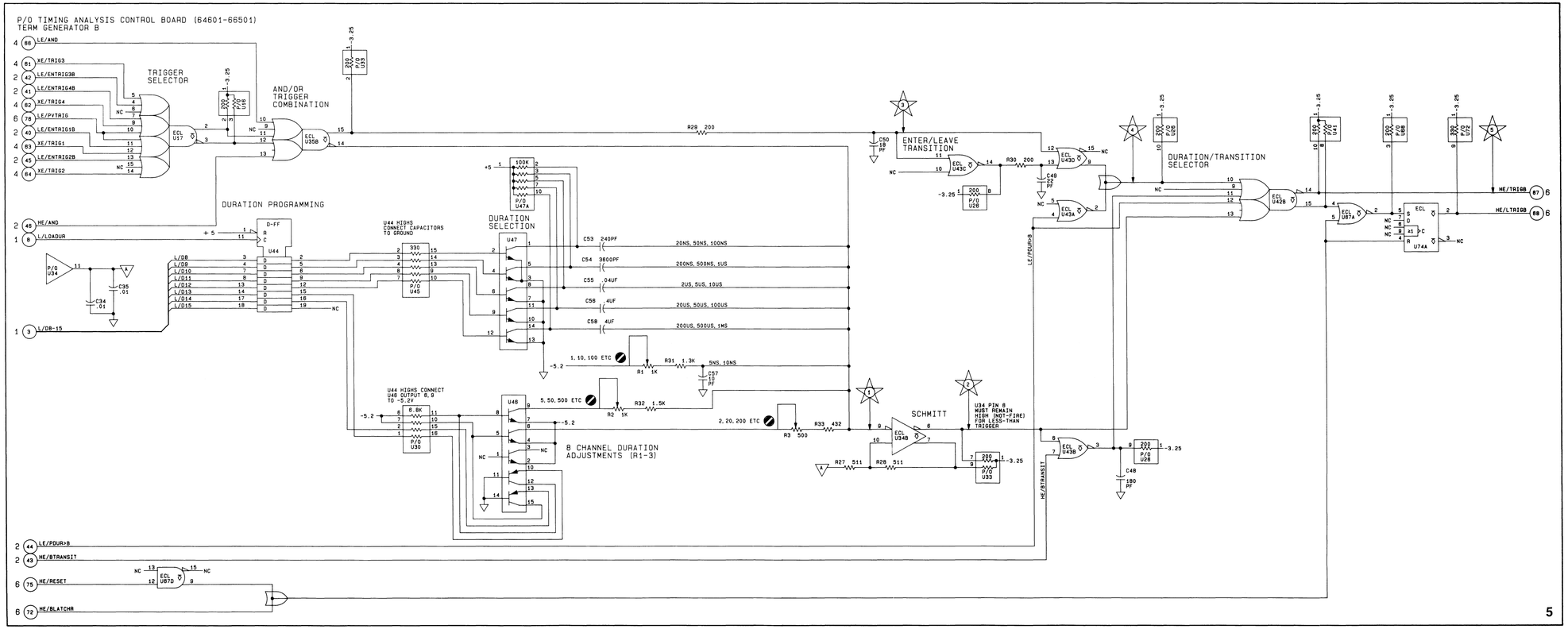


TERM GENERATORS



WAVEFORM	IC PIN	ENTERING	LEAVING	LESS THAN
1	U34-9			
2	U34-6			
3	U43-11,12			
4	U43-9			
5	U42-14			

XE/TRIG	HE/TRANSIT	LE/PDUR>	PATTERN MUST BE:
H	X	L	GREATER THAN SPECIFIED
H	L	H	LESS THAN SPECIFIED
H	H	H	TRANSITION LEAVING
L	H	H	TRANSITION ENTERING



ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr. Part No
U17	1820-0815	MC10121P
U34	1820-1320	MC10216P
U35,42	1820-1946	MC10117L
U43,67	1820-0802	MC10102P
U44	1820-1730	SN74LS273N
U46	1858-0054	
U47	1821-0002	CA3054
U74	1820-0817	MC10131P

PARTS ON THIS SCHEMATIC

C48-50,53-58
R1-3,27-33
U16,26,30,33,41,45,47A,68,72 (RESISTOR PACKS)

IC POWER SUPPLY CONFIGURATION

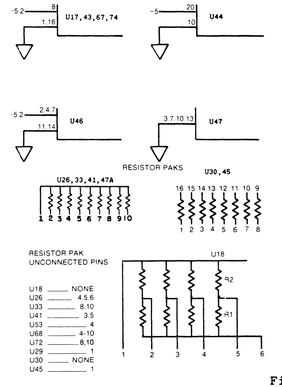
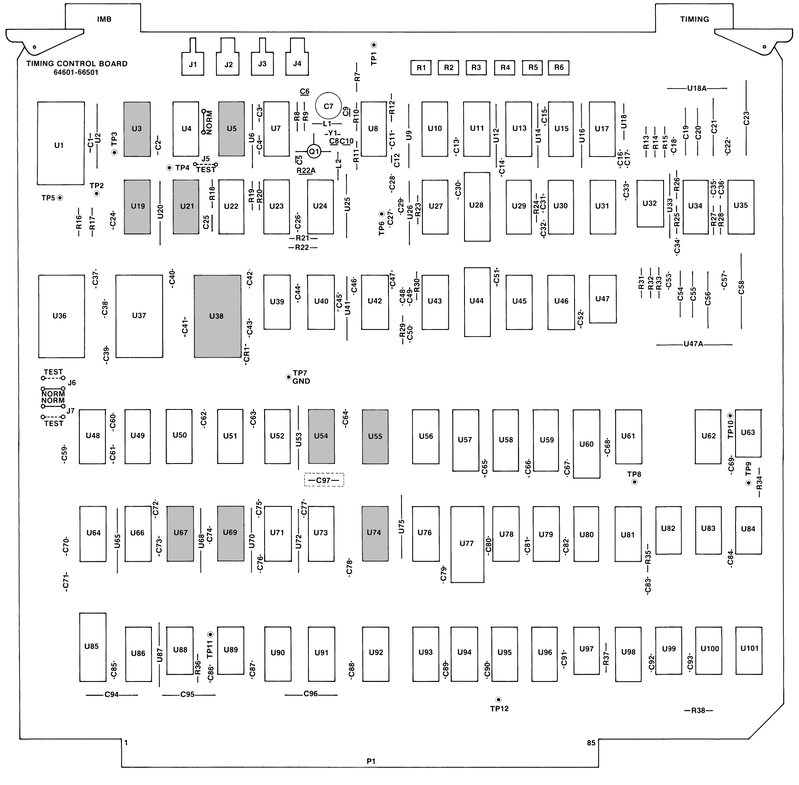
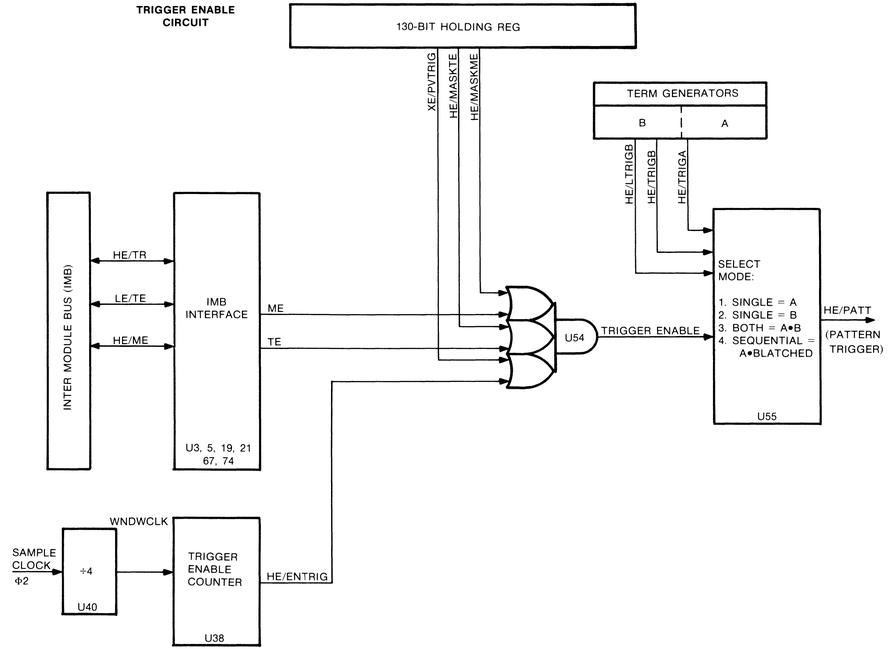
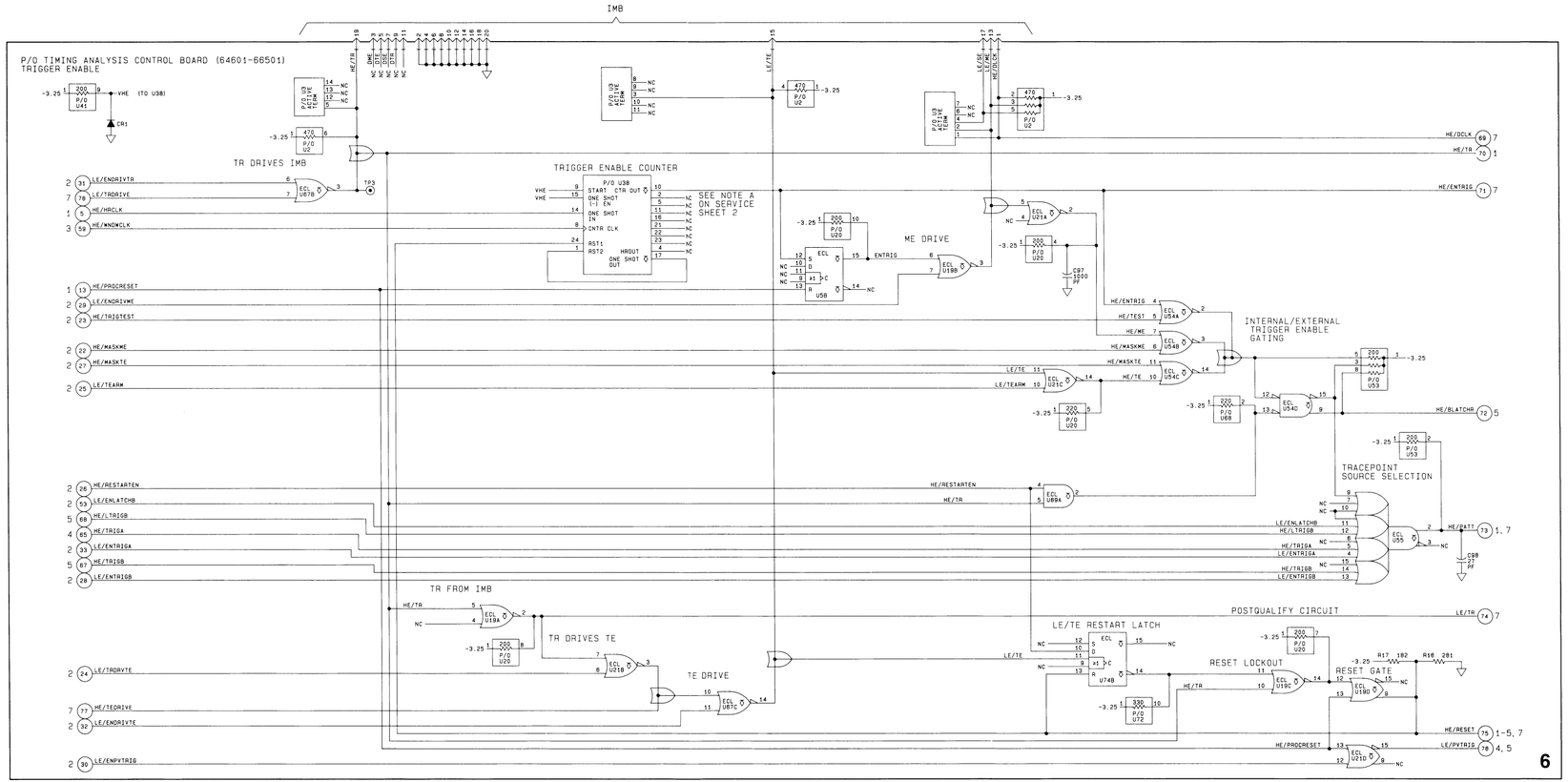


Figure 8-13.
Service Sheet 5
Term Generator B
CTL 8-33
CHANGE 1


IMB
TIMING
TIMING CONTROL BOARD
64601-66501
J1
J2
J3
J4
TP1
R1
R2
R3
R4
R5
R6
U18A
C6
C7
L1
L2
Y1
C8
C9
C10
Q1
C5
R22A
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
U30
U31
U32
U34
U35
TP2
TP3
TP4
TP5
TP6
J5
TEST
NORM
U36
U37
U38
U39
U40
U41
U42
U43
U44
U45
U46
U47
U47A
TP7
GND
J6
J7
U48
U49
U50
U51
U52
U53
U54
U55
U56
U57
U58
U59
U60
U61
U62
U63
TP8
TP9
TP10
U64
U66
U67
U69
U71
U73
U74
U76
U77
U78
U79
U80
U81
U82
U83
U84
U85
U86
U87
U88
U89
U90
U91
U92
U93
U94
U95
U96
U97
U98
U99
U100
U101
TP11
TP12
C94
C95
C96
C97
R38
P1
1
85


TRIGGER ENABLE CIRCUIT
130-BIT HOLDING REG
XE/PVTRIG
HE/MASKTE
HE/MASKME
TERM GENERATORS
B
I
A
HE/LTRIGB
HE/TRIGB
HE/TRIGA
INTER MODULE BUS (IMB)
HE/TR
LE/TE
HE/ME
IMB INTERFACE
U3, 5, 19, 21
67, 74
ME
TE
U54
TRIGGER ENABLE
SELECT MODE:
1. SINGLE = A
2. SINGLE = B
3. BOTH = A•B
4. SEQUENTIAL = A•BLATCHED
U55
HE/PATT
(PATTERN TRIGGER)
WNDWCLK
SAMPLE CLOCK
Φ2
÷4
U40
TRIGGER ENABLE COUNTER
U38
HE/ENTRIG



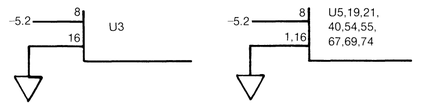
ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr. Part No.
U3	1820-2359	F10014PC
U5	1820-1225	MC10231P
U54,67,19,21	1820-0802	MC10102P
U55	1820-0815	MC10121P
U69	1820-1400	MC10104P
U74	1820-0817	MC10131P
U38	1NB4-5008	

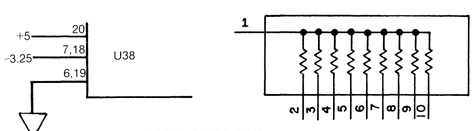
PARTS ON THIS SCHEMATIC

C97,98
R16,17
U2,20,41,53,68,72 (RESISTOR PACKS)

IC POWER SUPPLY CONFIGURATION



RESISTOR PAK U2,20,41,53,68,72



UNCONNECTED PINS

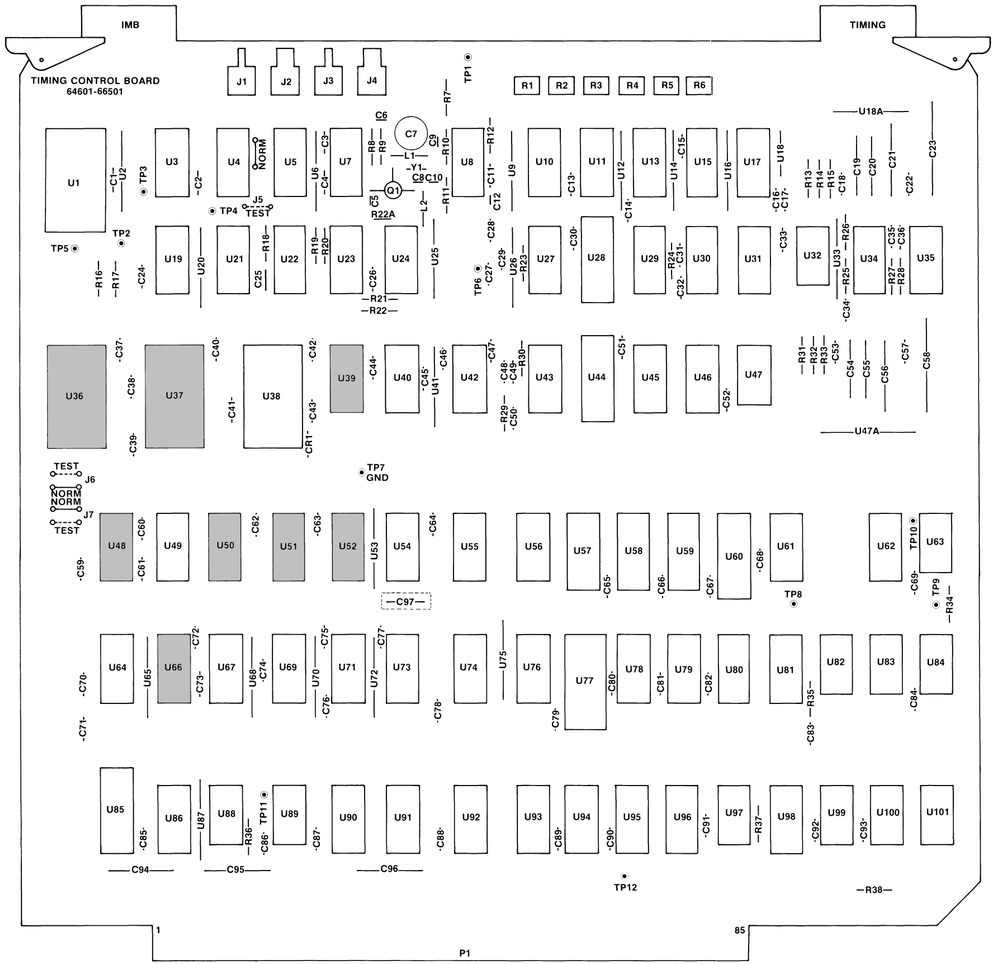
U2 _____ 7-10
U20 _____ NONE
U41 _____ 3,5
U53 _____ 4
U68 _____ 4-10
U72 _____ 8,10

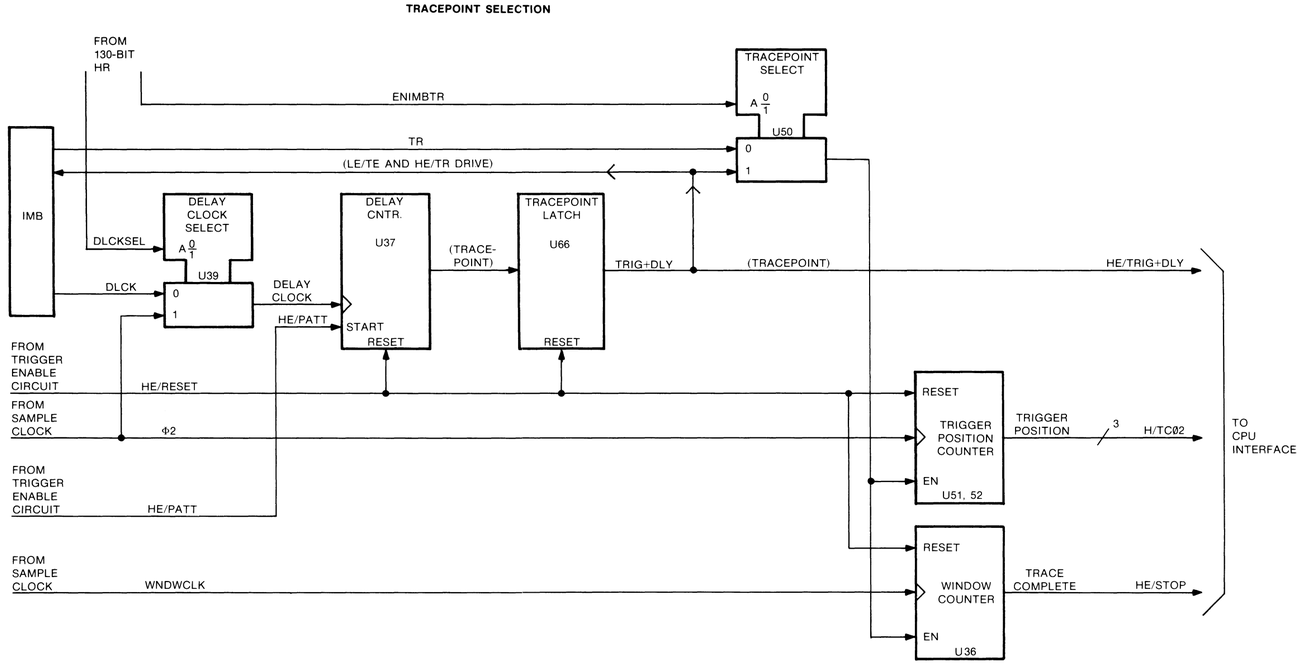
NOTE A

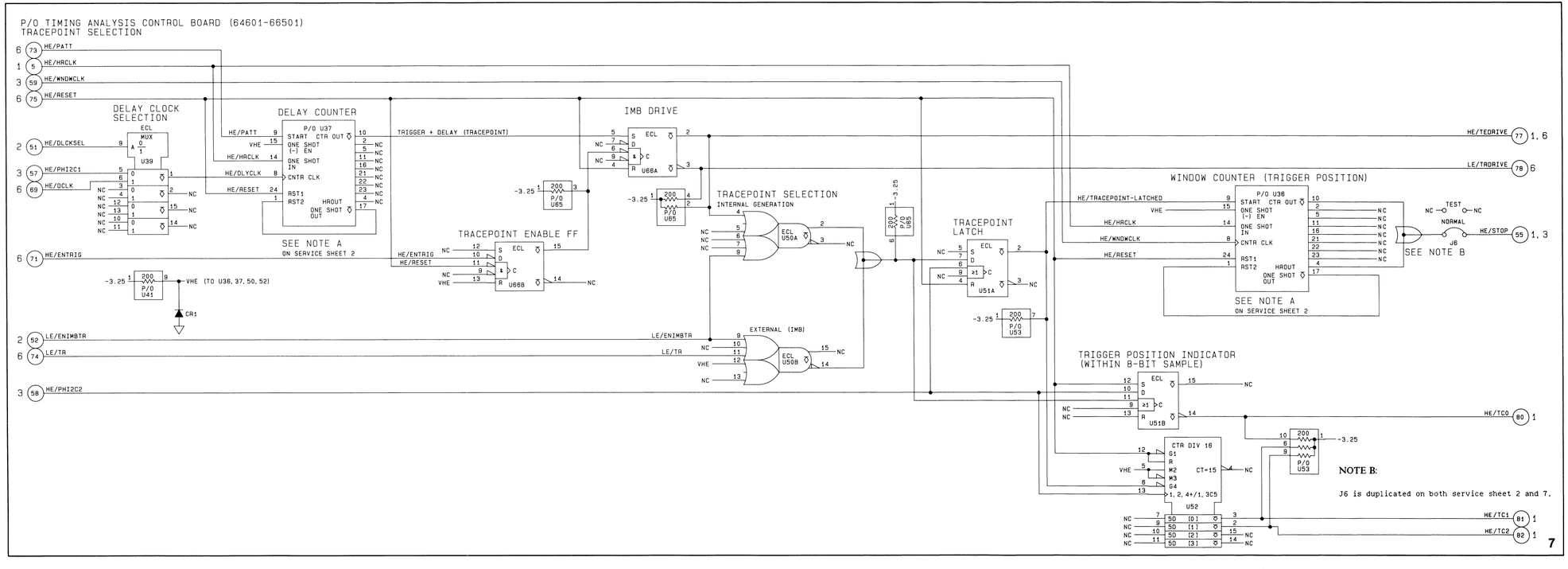
THE 25 BIT HOLDING REGISTER PART OF U38 IS SHOWN ON SHEET 2

Figure 8-14.
Service Sheet 6
Trigger Enable Circuit

CHANGE 1


IMB
TIMING
TIMING CONTROL BOARD
64601-66501
J1
J2
J3
J4
R1
R2
R3
R4
R5
R6
TP1
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U18A
C6
C7
C8
C9
C10
L1
L2
Y1
Q1
R22A
TP2
TP3
TP4
TP5
TP6
J5
NORM
TEST
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
U30
U31
U32
U33
U34
U35
U36
U37
U38
U39
U40
U41
U42
U43
U44
U45
U46
U47
U47A
TP7
GND
J6
J7
U48
U49
U50
U51
U52
U53
U54
U55
U56
U57
U58
U59
U60
U61
U62
U63
TP8
TP9
TP10
C97
U64
U65
U66
U67
U68
U69
U70
U71
U72
U73
U74
U75
U76
U77
U78
U79
U80
U81
U82
U83
U84
U85
U86
U87
U88
U89
U90
U91
U92
U93
U94
U95
U96
U97
U98
U99
U100
U101
TP11
TP12
C94
C95
C96
R38
1
85
P1


TRACEPOINT SELECTION
FROM 130-BIT HR
ENIMBTR
TRACEPOINT SELECT
A 0/1
U50
0
1
TR
(LE/TE AND HE/TR DRIVE)
IMB
DELAY CLOCK SELECT
A 0/1
U39
DLCKSEL
DLCK
0
1
DELAY CLOCK
HE/PATT
DELAY CNTR.
U37
START
RESET
(TRACE-POINT)
TRACEPOINT LATCH
U66
RESET
TRIG+DLY
(TRACEPOINT)
HE/TRIG+DLY
FROM TRIGGER ENABLE CIRCUIT
HE/RESET
FROM SAMPLE CLOCK
Φ2
FROM TRIGGER ENABLE CIRCUIT
HE/PATT
FROM SAMPLE CLOCK
WNDWCLK
RESET
TRIGGER POSITION COUNTER
EN
U51, 52
TRIGGER POSITION
3
H/TCØ2
RESET
WINDOW COUNTER
EN
U36
TRACE COMPLETE
HE/STOP
TO CPU INTERFACE



ICs ON THIS SCHEMATIC

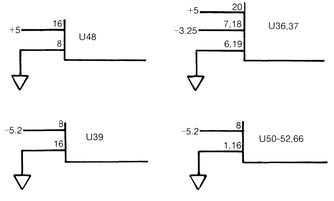
Ref Des	HP Part No.	Mfr. Part No.
U36,37	1NB4-5008	
U39	1820-1993	MC10158L
U48	1820-0780	DS8831N
U50	1820-1946	MC10117L
U51	1820-0817	MC10131P
U52	1820-1788	F10016DC
U66	1820-1944	MC10130L

PARTS ON THIS SCHEMATICS

J6

U53,65 (RESISTOR PACKS)

IC POWER SUPPLY CONFIGURATION

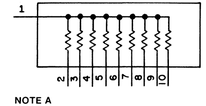


UNCONNECTED PINS

U53 _____ PIN 4

U65 _____ 5,7-10

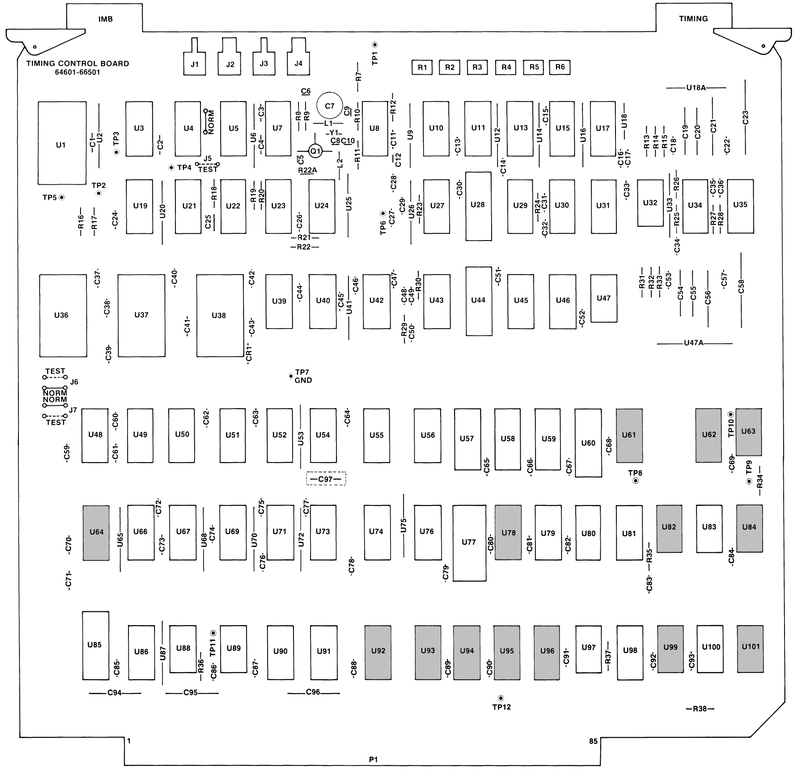
RESISTOR PAKS U53,65

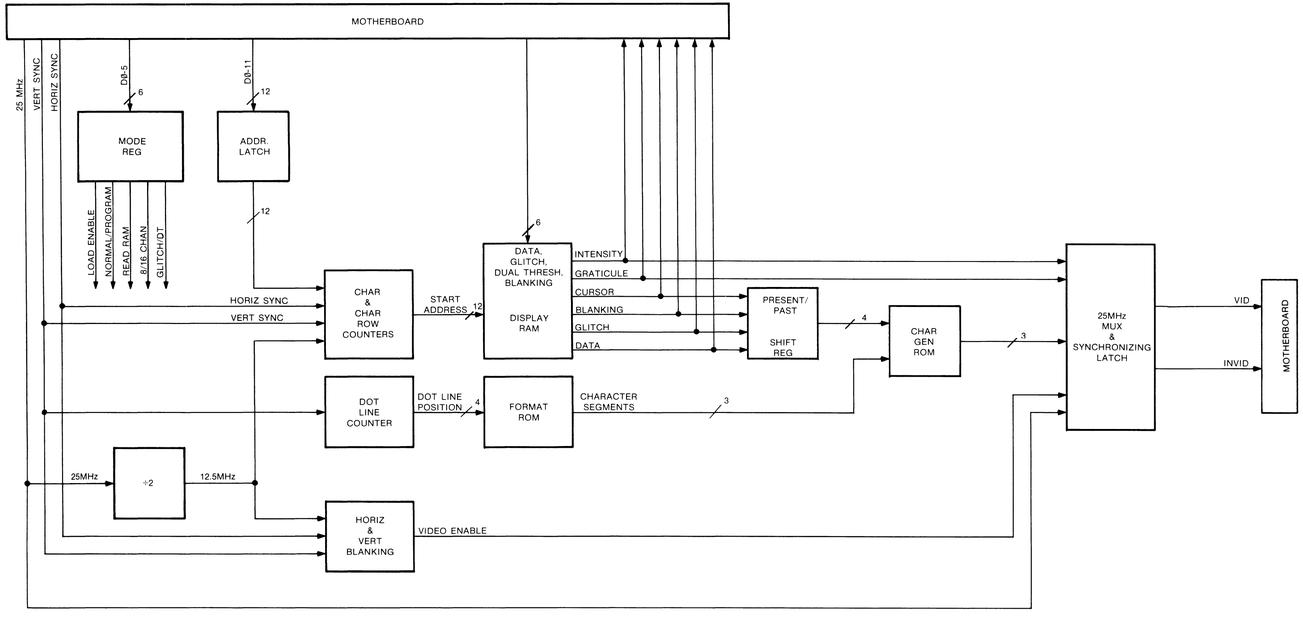


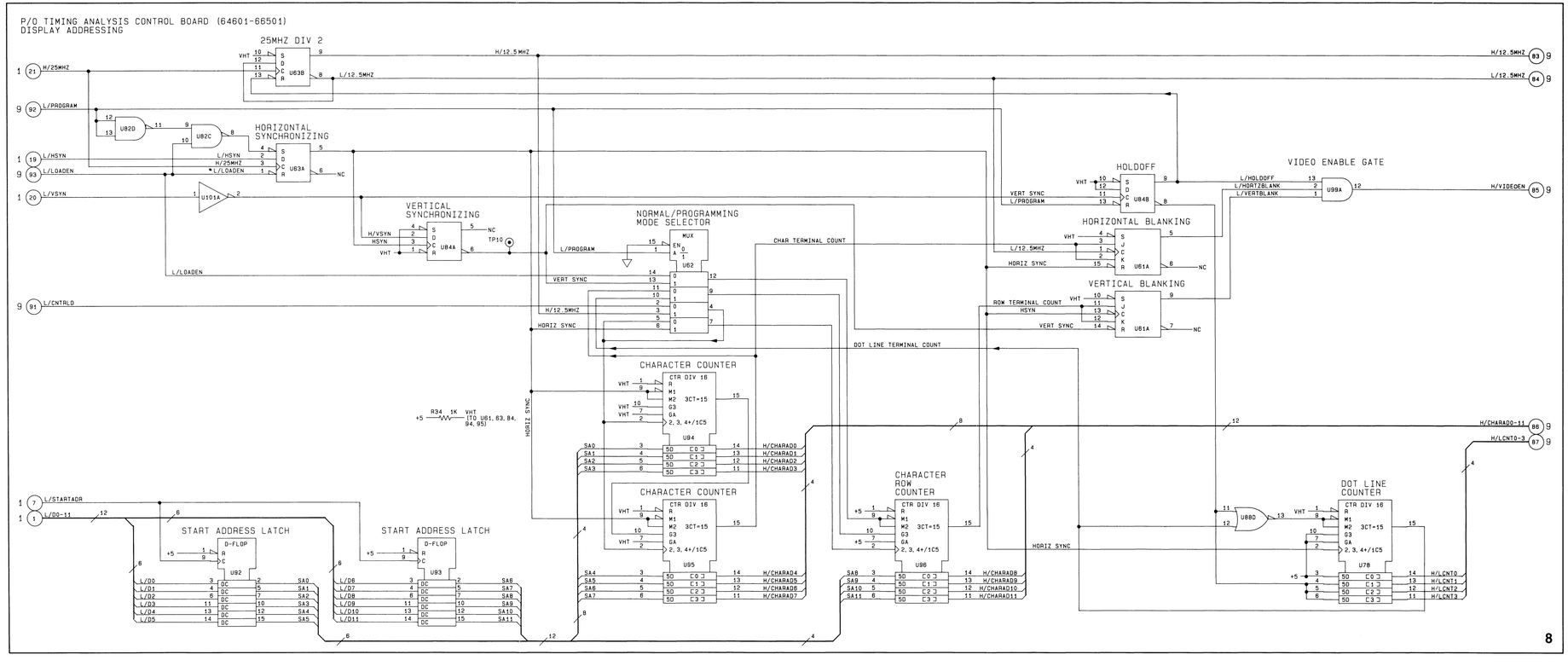
NOTE A

THE 25 BIT HOLDING REGISTER SECTIONS OF U36, U37 ARE SHOWN ON SHEET 2

Figure 8-15.
Service Sheet 7
Tracepoint Selection
CTL 8-37


IMB
TIMING
TIMING CONTROL BOARD
64601-66501
J1
J2
J3
J4
TP1
R1
R2
R3
R4
R5
R6
U1
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
U12
U13
U14
U15
U16
U17
U18
U18A
U19
U20
U21
U22
U23
U24
U25
U26
U27
U28
U29
U30
U31
U32
U33
U34
U35
U36
U37
U38
U39
U40
U41
U42
U43
U44
U45
U46
U47
U47A
U48
U49
U50
U51
U52
U53
U54
U55
U56
U57
U58
U59
U60
U61
U62
U63
U64
U65
U66
U67
U68
U69
U70
U71
U72
U73
U74
U75
U76
U77
U78
U79
U80
U81
U82
U83
U84
U85
U86
U87
U88
U89
U90
U91
U92
U93
U94
U95
U96
U97
U98
U99
U100
U101
TP2
TP3
TP4
TP5
TP6
TP7
GND
TP8
TP9
TP10
TP11
TP12
J5
TEST
J6
NORM
J7
Q1
L1
L2
Y1
C6
C7
C8
C9
C10
C97
C94
C95
C96
R22A
R38
1
85
P1


MOTHERBOARD
25 MHz
VERT SYNC
HORIZ SYNC
D/B-5
D/B-11
6
12
MODE REG
ADDR. LATCH
LOAD ENABLE
NORMAL/PROGRAM
READ RAM
8/16 CHAN
GLITCH/DT
CHAR & CHAR ROW COUNTERS
START ADDRESS
DATA, GLITCH, DUAL THRESH, BLANKING
DISPLAY RAM
INTENSITY
GRATICULE
CURSOR
BLANKING
GLITCH
DATA
PRESENT/ PAST SHIFT REG
CHAR GEN ROM
25MHz MUX & SYNCHRONIZING LATCH
VID
INVID
MOTHERBOARD
DOT LINE COUNTER
DOT LINE POSITION
FORMAT ROM
CHARACTER SEGMENTS
25MHz
÷2
12.5MHz
HORIZ & VERT BLANKING
VIDEO ENABLE



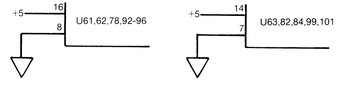
ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr. Part No.
U61,64	1820-0629	SN74S112N
U62	1820-1077	SN74S157N
U63,84	1820-0693	SN74S74N
U78,96	1820-1430	SN74LS161AN
U82	1820-1197	SN74LS00N
U92,93	1820-1196	SN74LS174N
U94,95	1820-1475	93S16DC
U99	1820-0686	SN74S11N
U101	1820-0683	SN74S04N

PARTS ON THIS SCHEMATIC

R38

IC POWER SUPPLY CONFIGURATION



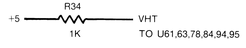
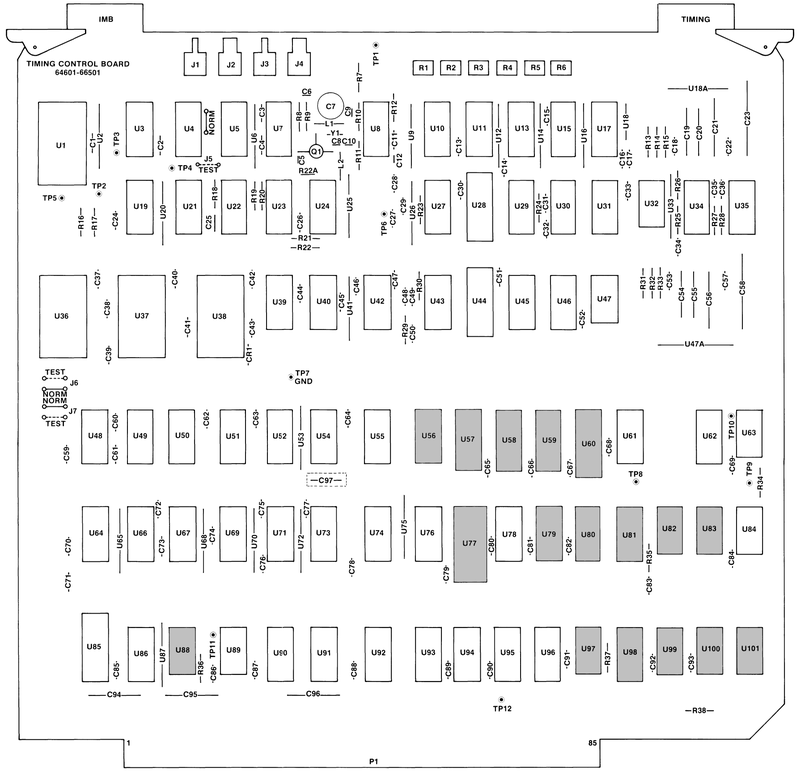


Figure 8-16.
Service Sheet 8
Display Addressing
CTL 8-39


IMB
TIMING
TIMING CONTROL BOARD
64601-66501
J1
J2
J3
J4
R1
R2
R3
R4
R5
R6
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GND
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TEST
NORM
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J6
J7
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Q1
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C97
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C95
C96
R38
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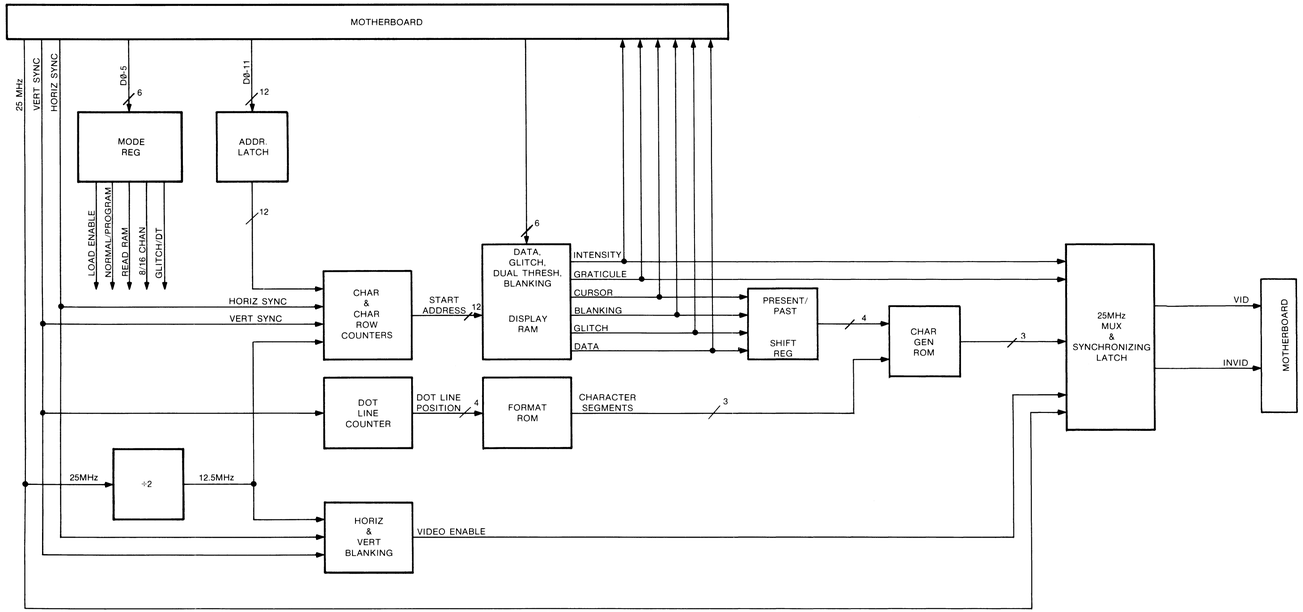
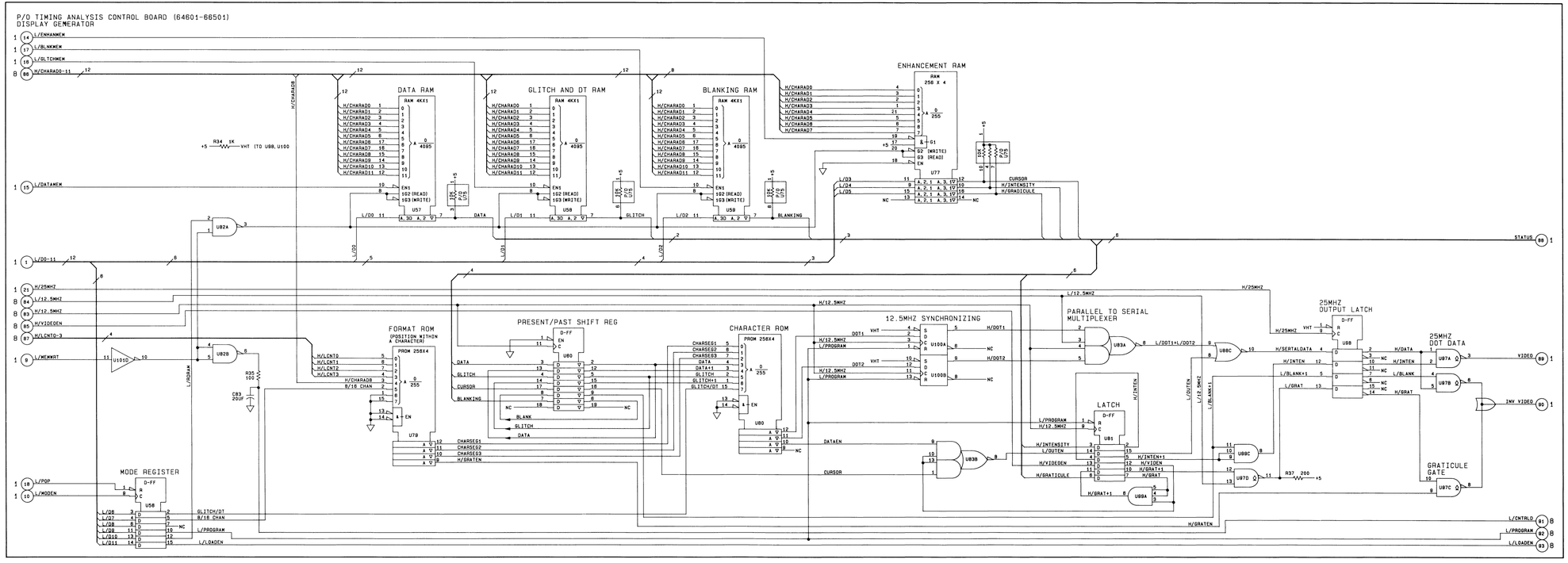

MOTHERBOARD
25 MHz
VERT SYNC
HORIZ SYNC
D8-5
6
D8-11
12
MODE REG
ADDR. LATCH
LOAD ENABLE
NORMAL/PROGRAM
READ RAM
8/16 CHAN
GLITCH/DT
12
6
DATA, GLITCH, DUAL THRESH, BLANKING
DISPLAY RAM
INTENSITY
GRATICULE
CURSOR
BLANKING
GLITCH
DATA
HORIZ SYNC
VERT SYNC
CHAR & CHAR ROW COUNTERS
START ADDRESS
12
PRESENT/ PAST
SHIFT REG
4
CHAR GEN ROM
3
25MHz MUX & SYNCHRONIZING LATCH
VID
INVID
MOTHERBOARD
DOT LINE COUNTER
DOT LINE POSITION
4
FORMAT ROM
CHARACTER SEGMENTS
3
25MHz
÷2
12.5MHz
HORIZ & VERT BLANKING
VIDEO ENABLE



ICs ON THIS SCHEMATIC

Ref Des	HP Part No.	Mfr. Part No.
U56	1820-1196	SN74LS174N
U57-59	1818-1596	HM6147P-3
U60	1820-1677	SN74S374N
U77	1816-1308	93L422 PC
U79	64601-10002	
U80	64601-10001	
U81	1820-1076	SN74S174N
U82	1820-1197	SN74LS00N
U83	1820-1158	SN74S51N
U88	1820-1322	SN74S02N
U97	1820-1451	SN74S38N
U98	1820-1191	SN74S175N
U99	1820-0686	SN74S11N
U100	1820-0693	SN74S74N
U101	1820-0683	SN74S04N

PARTS ON THIS SCHEMATIC

C83
R35,37
U75 (RESISTOR PACK)

IC POWER SUPPLY CONFIGURATION

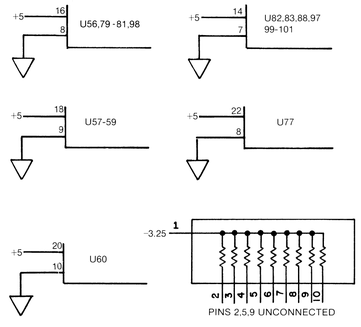


Figure 8-17.
Service Sheet 9
Display Driver
CTL 8-41

SALES & SUPPORT OFFICES

Arranged alphabetically by country

Product Line Sales/Support Key

Key	Product Line
A	Analytical
CM	Components
C	Computer Systems Sales only
CH	Computer Systems Hardware Sales and Services
CS	Computer Systems Software Sales and Services
E	Electronic Instruments & Measurement Systems
M	Medical Products
MP	Medical Products Primary SRO
MS	Medical Products Secondary SRO
P	Personal Computation Products
*	Sales only for specific product line
**	Support only for specific product line

IMPORTANT: These symbols designate general product line capability. They do not insure sales or support availability for all products within a line, at all locations. Contact your local sales office for information regarding locations where HP support is available for specific products.

HP distributors are printed in italics.

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Empresa Técnica de Equipamentos
R. Barbosa Rodrigues, 41-I DT.
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Avenida Santa Fe 2035
Martinez 1640 **BUENOS AIRES**
Tel: 798-5735, 792-1293
Telex: 17595 BIONAR
Cable: HEWPACKARG
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Biotron S.A.C.I.M. e I.
Av Paseo Colon 221, Piso 9
1399 ***BUENOS AIRES***
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Telex: 17595 BIONAR
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153 Greenhill Road
PARKSIDE, S.A. 5063
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Telex: 82536
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Hewlett-Packard Australia Ltd.
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Canberra, Australia Capital Territory Office

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NORTH RYDE, N.S.W. 2113
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Verkaufsburo Graz
A-8052 **GRAZ**
Tel: 291-5-66
Telex: 32375
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Lieblgasse 1
P.O. Box 72
A-1222 **VIENNA**
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Telex: 134425 HEPA A
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BAHRAIN
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Telex: 84419
P

Wael Pharmacy
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Tel: 256123
Telex: 8550 WAEL BN
E,M

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Blvd de la Woluwe, 100
Woluwedal
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Alphaville
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Telex: (011) 33872 HPBR-BR
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Telex: 021-21905 HPBR-BR
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11620A-168th Street
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MONCTON, New Brunswick E2B 2VQ
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900 Windmill Road
DARTMOUTH, Nova Scotia B2Y 3Z6
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2670 Queensview Dr.
OTTAWA, Ontario K2B 8K1
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WILLOWDALE, Ontario M2J 1R5
Tel: (416) 499-9333
CH

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17500 South Service Road
Trans-Canada Highway
KIRKLAND, Quebec H9J 2M5
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Tel: (418) 687-4570
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Arturo Buhrle 065
Casilla 16475
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Tel: 222-0222
Telex: Public Booth 440001
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Av. Rodrigo de Araya 1045
Casilla 256-V
SANTIAGO 21
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Telex: 240-565 OLYMP CL
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CHINA, People's Republic of

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1A Lane 2, Luchang St.
Beiwei Rd., Xuanwu District
BEIJING
Tel: 33-1947, 33-7426
Telex: 22601 CTSHP CN
Cable: 1920
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H. A. Langebaek & Kier S.A.
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Apartado Aereo 6287
BOGOTA 1, D.E.
Tel: 212-1466
Telex: 44400 INST CO
Cable: AARIS Bogota
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Cientifica Costarricense S.A.
Avenida 2, Calle 5
San Pedro de Montes de Oca
Apartado 10159
SAN JOSÉ
Tel: 24-38-20, 24-08-19
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Telerexa Ltd.
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14C Stassinos Avenue
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Tel: 62698
Telex: 2894 LEVIDO CY
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DK-8240 **RISSKOV**
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Telex: 37409 hpas dk
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Juan Tomás Mejiá y Cotes No. 60
Arroyo Hondo
SANTO DOMINGO
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Telex: 4510 ARENTA DR (RCA)
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Telex: 2548 CYEDE ED
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Robles 625
Casilla 3590
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Tel: 545-250, 545-122
Telex: 2485 HOSPTL ED
Cable: HOSPITALAR-Quito
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Kasr-el-Aini
CAIRO
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Telex: IEA UN 93830
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Informatic For Systems
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CAIRO
Tel: 759006
Telex: 93938 FRANK UN
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Tel: 650021
Telex: 93337 EGPOR
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SAN SALVADOR
Tel: 26-6858, 26-6868
Telex: 20539 EPISA
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Arranged alphabetically by country

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Telex: 9100
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SF-40720-72 **JYVASKYLA**
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Kainvuntie 1-C
SF-90140-14 **OULU**
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F-13763 Les Milles Cedex
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Avenue du Président JF Kennedy
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G. Gerardos
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ATHENS
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Telex: 221871
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GUATEMALA CITY
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A,CH,CM,CS,E,M,P

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E,CH,CS,P

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Wing On Centre, 28th Floor
Connaught Road, C.
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A,M

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Hafnarnvoli-Tryggvagotu
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IS-REYKJAVIK
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M

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Computer products are sold through Blue Star Ltd. All computer repairs and maintenance service is done through Computer Maintenance Corp.

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A,M

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414/2 Vir Savarkar Marg
Prabhadevi
***BOMBAY** 400 025*
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Telex: 011-4093
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*Alkapuri, **BORODA**, 390 005*
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Telex: 021-7655
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A,M

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133 Kodambakkam High Road
***MADRAS** 600 034*
Tel: 82057
Telex: 041-379
Cable: BLUESTAR
A,M

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91 Nehru Place
***NEW DELHI** 110 024*
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Telex: 031-2463
Cable: BLUESTAR
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Cable: BLUE STAR
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Blue Star Ltd.
2-2-47/1108 Bolarum Rd.
***SECUNDERABAD** 500 003*
Tel: 72057
Telex: 0155-459
Cable: BLUEFROST
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Blue Star Ltd.
T.C. 7/603 Poornima
Maruthankuzhi
***TRIVANDRUM** 695 013*
Tel: 65799
Telex: 0884-259
Cable: BLUESTAR
E

Computer Maintenance Corporation Ltd.
115, Sarojini Devi Road
***SECUNDERABAD** 500 003*
Tel: 310-184, 345-774
Telex: 031-2960
*CH***

INDONESIA

BERCA Indonesia P.T.
P.O.Box 496/JKT.
Jl. Abdul Muis 62
JAKARTA
Tel: 373009
Telex: 46748 BERSAL IA
Cable: BERSAL JAKARTA
P

BERCA Indonesia P.T.
P.O.Box 2497/Jkt Antara Bldg.,
17th Floor
Jl. Medan Merdeka Selatan 17
JAKARTA-PUSAT
Tel: 21-344-181
Telex: BERSAL IA
A,CS,E,M

BERCA Indonesia P.T.
P.O. Box 174/SBY.
Jl. Kutei No. 11
SURABAYA
Tel: 68172
Telex: 31146 BERSAL SB
Cable: BERSAL-SURABAYA
A,E,M,P*

IRAQ

Hewlett-Packard Trading S.A.
Service Operation
Al Mansoor City 9B/3/7
BAGHDAD
Tel: 551-49-73
Telex: 212-455 HEPAIRAQ IK
CH,CS

SALES & SUPPORT OFFICES

Arranged alphabetically by country

IRELAND
Hewlett-Packard Ireland Ltd.
82/83 Lower Leeson Street
DUBLIN 2
Tel: (1) 60 88 00
Telex: 30439
A,CH,CM,CS,E,M,P

Cardiac Services Ltd.
Kilmore Road
Artane
DUBLIN 5
Tel: (01) 351820
Telex: 30439
M

ISRAEL
Eldan Electronic Instrument Ltd.
P.O.Box 1270
JERUSALEM 91000
16, Ohaliav St.
JERUSALEM 94467
Tel: 533 221, 553 242
Telex: 25231 AB/PAKRD IL
A

Electronics Engineering Division
Motorola Israel Ltd.
16 Kremenetski Street
P.O. Box 25016
TEL-AVIV 67899
Tel: 3-338973
Telex: 33569 Motil IL
Cable: BASTEL Tel-Aviv
CH,CM,CS,E,M,P

ITALY
Hewlett-Packard Italiana S.p.A
Traversa 99C
Via Giulio Petroni, 19
I-70124 **BARI**
Tel: (080) 41-07-44
M

Hewlett-Packard Italiana S.p.A.
Via Martin Luther King, 38/111
I-40132 **BOLOGNA**
Tel: (051) 402394
Telex: 511630
CH,E,MS

Hewlett-Packard Italiana S.p.A.
Via Principe Nicola 43G/C
I-95126 **CATANIA**
Tel: (095) 37-10-87
Telex: 970291
C,P

Hewlett-Packard Italiana S.p.A.
Via G. Di Vittorio 9
I-20063 **CERNUSCO SUL NAVIGLIO**
Tel: (2) 903691
Telex: 334632
A,CH,CM,CS,E,MP,P

Hewlett-Packard Italiana S.p.A.
Via Nuova San Rocco a
Capodimonte, 62/A
I-80131 **NAPLES**
Tel: (081) 7413544
Telex: 710698
A,CH,E

Hewlett-Packard Italiana S.p.A.
Viale G. Modugno 33
I-16156 **GENOVA PEGLI**
Tel: (010) 68-37-07
Telex: 215238
E,C

Hewlett-Packard Italiana S.p.A.
Via Turazza 14
I-35100 **PADOVA**
Tel: (049) 664888
Telex: 430315
A,CH,E,MS

Hewlett-Packard Italiana S.p.A.
Viale C. Pavese 340
I-00144 **ROMA**
Tel: (06) 54831
Telex: 610514
A,CH,CM,CS,E,MS,P*

Hewlett-Packard Italiana S.p.A.
Corso Svizzera, 184
I-10149 **TORINO**
Tel: (011) 74 4044
Telex: 221079
CH,E

JAPAN
Yokogawa-Hewlett-Packard Ltd.
152-1, Onna
000 **ATSUGI,** Kanagawa, 243
Tel: (0462) 28-0451
CM,C*,E

Yokogawa-Hewlett-Packard Ltd.
Towa Building
2-3, Kaigan-dori, 2 Chome Chuo-ku
KOBE, 650
Tel: (078) 392-4791
C,E

Yokogawa-Hewlett-Packard Ltd.
Kumagaya Asahi 82 Bldg
3-4 Tsukuba
KUMAGAYA, Saitama 360
Tel: (0485) 24-6563
CH,CM,E

Yokogawa-Hewlett-Packard Ltd.
Asahi Shinbun Daiichi Seimei Bldg.
4-7, Hanabata-cho
KUMAMOTO,860
Tel: (0963) 54-7311
CH,E

Yokogawa-Hewlett-Packard Ltd.
Shin-Kyoto Center Bldg.
614, Higashi-Shiokoji-cho
Karasuma-Nishiiru
Shiokoji-dori, Shimogyo-ku
KYOTO, 600
Tel: 075-343-0921
CH,E

Yokogawa-Hewlett-Packard Ltd.
Mito Mitsui Bldg
4-73, Sannomaru, 1 Chome
MITO, Ibaragi 310
Tel: (0292) 25-7470
CH,CM,E

Yokogawa-Hewlett-Packard Ltd.
Sumitomo Seimei 14-9 Bldg.
Meieki-Minami, 2 Chome
Nakamura-ku
NAGOYA, 450
Tel: (052) 571-5171
CH,CM,CS,E,MS

Yokogawa-Hewlett-Packard Ltd.
Chuo Bldg.,
4-20 Nishinakajima, 5 Chome
Yodogawa-ku
OSAKA, 532
Tel: (06) 304-6021
Telex: YHPOSA 523-3624
A,CH,CM,CS,E,MP,P*

Yokogawa-Hewlett-Packard Ltd.
27-15, Yabe, 1 Chome
SAGAMIHARA Kanagawa, 229
Tel: 0427 59-1311

Yokogawa-Hewlett-Packard Ltd.
Daiichi Seimei Bldg.
7-1, Nishi Shinjuku, 2 Chome
Shinjuku-ku,**TOKYO** 160
Tel: 03-348-4611-5
CH,E

Yokogawa-Hewlett-Packard Ltd.
29-21 Takaido-Higashi, 3 Chome
Suginami-ku **TOKYO** 168
Tel: (03) 331-6111
Telex: 232-2024 YHPTOK
A,CH,CM,CS,E,MP,P*

Yokogawa-Hewlett-Packard Ltd.
Daiichi Asano Building
2-8, Odori, 5 Chome
UTSUNOMIYA, Tochigi 320
Tel: (0286) 25-7155
CH,CS,E

Yokogawa-Hewlett-Packard Ltd.
Yasuda Seimei Nishiguchi Bldg.
30-4 Tsuruya-cho, 3 Chome
YOKOHAMA221
Tel: (045) 312-1252
CH,CM,E

JORDAN
Mouasher Cousins Company
P.O. Box 1387
AMMAN
Tel: 24907, 39907
Telex: 21456 SABCO JO
CH,E,M,P

KENYA
ADCOM Ltd., Inc., Kenya
P.O.Box 30070
NAIROBI
Tel: 331955
Telex: 22639
E,M

KOREA
Samsung Electronics Computer Division
76-561 Yeoksam-Dong
Kwangnam-Ku
C.P.O. Box 2775
SEOUL
Tel: 555-7555, 555-5447
Telex: K27364 SAMSAN
A,CH,CM,CS,E,M,P

KUWAIT
Al-Khaldiya Trading & Contracting
P.O. Box 830 Safat
KUWAIT
Tel: 42-4910, 41-1726
Telex: 22481 Areeg kt
CH,E,M

Photo & Cine Equipment
P.O. Box 270 Safat
KUWAIT
Tel: 42-2846, 42-3801
Telex: 22247 Matin kt
P

LEBANON
G.M. Dolmadjian
Achrafieh
P.O. Box 165.167
BEIRUT
Tel: 290293
*MP***

LUXEMBOURG
Hewlett-Packard Belgium S.A./N.V.
Blvd de la Woluwe, 100
Woluwedal
B-1200 **BRUSSELS**
Tel: (02) 762-32-00
Telex: 23-494 paloben bru
A,CH,CM,CS,E,MP,P

MALAYSIA
Hewlett-Packard Sales (Malaysia)
Sdn. Bhd.
1st Floor, Bangunan British
American
Jalan Semantan, Damansara Heights
KUALA LUMPUR 23-03
Tel: 943022
Telex: MA31011
A,CH,E,M,P*

Protel Engineering
P.O.Box 1917
Lot 6624, Section 64
23/4 Pending Road
Kuching, ***SARAWAK***
Tel: 36299
Telex: MA 70904 PROTEL
Cable: PROTELENG
A,E,M

MALTA
Philip Toledo Ltd.
Notabile Rd.
MRIEHEL
Tel: 447 47, 455 66
Telex: Media MW 649
P

MEXICO
Hewlett-Packard Mexicana, S.A.
de C.V.
Av. Periferico Sur No. 6501
Tepepan, Xochimilco
MEXICO D.F. 16020
Tel: 676-4600
Telex: 17-74-507 HEWPACK MEX
A,CH,CS,E,MS,P

Hewlett-Packard Mexicana, S.A.
de C.V.
Ave. Colonia del Valle #409
Col. del Valle
Municipio de Garza Garcia
MONTERREY, N.L.
Tel: 78 42 41
Telex: 038 410
CH

ECISA
José Vasconcelos No. 218
Col. Condesa Deleg. Cuauhtémoc
***MEXICO** D.F. 06140*
Tel: 553-1206
Telex: 17-72755 ECE ME
M

MOROCCO
Dolbeau
81 rue Karatchi
CASABLANCA
Tel: 3041-82, 3068-38
Telex: 23051, 22822
E

Gerep
2 rue d'Agadir
Boite Postale 156
CASABLANCA
Tel: 272093, 272095
Telex: 23 739
P

NETHERLANDS
Hewlett-Packard Nederland B.V.
Van Heuven Goedhartlaan 121
NL 1181KK **AMSTELVEEN**
P.O. Box 667
NL1180 AR **AMSTELVEEN**
Tel: (020) 47-20-21
Telex: 13 216 HEPA NL
A,CH,CM,CS,E,MP,P

Hewlett-Packard Nederland B.V.
Bongerd 2
NL 2906VK **CAPELLE, A/D IJSSEL**
P.O. Box 41
NL 2900AA **CAPELLE, A/D IJSSEL**
Tel: (10) 51-64-44
Telex: 21261 HEPAC NL
A,CH,CS,E

NEW ZEALAND
Hewlett-Packard (N.Z.) Ltd.
169 Manukau Road
P.O. Box 26-189
Epsom, **AUCKLAND**
Tel: 687-159
Cable: HEWPACK Auckland
CH,CM,E,P*

Hewlett-Packard (N.Z.) Ltd.
4-12 Cruickshank Street
Kilbirnie, **WELLINGTON 3**
P.O. Box 9443
Courtenay Place, **WELLINGTON 3**
Tel: 877-199
Cable: HEWPACK Wellington
CH,CM,E,P

Northrop Instruments & Systems Ltd.
369 Khyber Pass Road
P.O. Box 8602
AUCKLAND
Tel: 794-091
Telex: 60605
A,M

Northrop Instruments & Systems Ltd.
110 Mandeville St.
P.O. Box 8388
CHRISTCHURCH
Tel: 486-928
Telex: 4203
A,M

Northrop Instruments & Systems Ltd.
Sturdee House
85-87 Ghuznee Street
P.O. Box 2406
WELLINGTON
Tel: 850-091
Telex: NZ 3380
A,M

NORTHERN IRELAND
See United Kingdom

NORWAY
Hewlett-Packard Norge A/S
Folke Bernadottes vei 50
P.O. Box 3558
N-5033 **FYLLINGSDALEN** (Bergen)
Tel: (05) 16-55-40
Telex: 16621 hpnas n
CH,CS,E,MS

Hewlett-Packard Norge A/S
Österndalen 18
P.O. Box 34
N-1345 **ÖSTERÅS**
Tel: (02) 17-11-80
Telex: 16621 hpnas n
A,CH,CM,CS,E,M,P

OMAN
Khimjil Ramdas
P.O. Box 19
MUSCAT
Tel: 722225, 745601
Telex: 3289 BROKER MB MUSCAT
P

Suhail & Saud Bahwan
P.O.Box 169
MUSCAT
Tel: 734 201-3
Telex: 3274 BAHWAN MB

PAKISTAN
Mushko & Company Ltd.
1-B, Street 43
Sector F-8/1
ISLAMABAD
Tel: 26875
Cable: FEMUS Rawalpindi
A,E,M

Mushko & Company Ltd.
Oosman Chambers
Abdullah Haroon Road
***KARACHI** 0302*
Tel: 524131, 524132
Telex: 2894 MUSKO PK
Cable: COOPERATOR Karachi
*A,E,M,P**

PANAMA
Electrónico Balboa, S.A.
Calle Samuel Lewis, Ed. Alfa
Apartado 4929
PANAMA 5
Tel: 64-2700
Telex: 3483 ELECTRON PG
A,CM,E,M,P

4 SALES & SUPPORT OFFICES

Arranged alphabetically by country

PERU

Cía Electro Médica S.A.
Los Flamencos 145, San Isidro
Casilla 1030
***LIMA** 1*
Tel: 41-4325, 41-3703
Telex: Pub. Booth 25306
CM,E,M,P

PHILIPPINES

The Online Advanced Systems Corporation
Rico House, Amorsolo Cor. Herrera Street
Legaspi Village, Makati
P.O. Box 1510
*Metro **MANILA***
Tel: 85-35-81, 85-34-91, 85-32-21
Telex: 3274 ONLINE
A,CH,CS,E,M

Electronic Specialists and Proponents Inc.
690-B Epifanio de los Santos Avenue
*Cubao, **QUEZON CITY***
P.O. Box 2649 Manila
Tel: 98-96-81, 98-96-82, 98-96-83
Telex: 40018, 42000 ITT GLOBE MACKAY BOOTH
P

PORTUGAL

Mundinter
Intercambio Mundial de Comércio S.A.R.L.
P.O. Box 2761
Avenida Antonio Augusto de Aguiar 138
P-LISBON
Tel: (19) 53-21-31, 53-21-37
Telex: 16691 munter p
M

Soquimica
Av. da Liberdade, 220-2
*1298 **LISBOA** Codex*
Tel: 56 21 81/2/3
Telex: 13316 SABASA
P

Telectra-Empresa Técnica de Equipmentos Eléctricos S.A.R.L.
Rua Rodrigo da Fonseca 103
P.O. Box 2531
***P-LISBON** 1*
Tel: (19) 68-60-72
Telex: 12598
CH,CS,E,P

PUERTO RICO

Hewlett-Packard Puerto Rico
P.O. Box 4407
CAROLINA, Puerto Rico 00628
Calle 272 Edificio 203
Urb. Country Club
RIO PIEDRAS, Puerto Rico
Tel: (809) 762-7255
A,CH,CS

QATAR

Computearbia
P.O. Box 2750
DOHA
Tel: 883555
Telex: 4806 CHPARB
P

Eastern Technical Services
P.O.Box 4747
DOHA
Tel: 329 993
Telex: 4156 EASTEC DH

Nasser Trading & Contracting
P.O.Box 1563
DOHA
Tel: 22170, 23539
Telex: 4439 NASSER DH
M

SAUDI ARABIA

Modern Electronic Establishment
Hewlett-Packard Division
P.O. Box 281
Thuobah
AL-KHOBAR
Tel: 864-46 78
Telex: 671 106 HPMEEK SJ
Cable: ELECTA AL-KHOBAR
CH,CS,E,M,P

Modern Electronic Establishment
Hewlett-Packard Division
P.O. Box 1228
Redec Plaza, 6th Floor
JEDDAH
Tel: 644 38 48
Telex: 4027 12 FARNAS SJ
Cable: ELECTA JEDDAH
CH,CS,E,M,P

Modern Electronic Establishment
Hewlett-Packard Division
P.O.Box 2728
RIYADH
Tel: 491-97 15, 491-63 87
Telex: 202049 MEERYD SJ
CH,CS,E,M,P

SCOTLAND

See United Kingdom

SINGAPORE

Hewlett-Packard Singapore (Sales) Pte. Ltd.
P.O. Box 58 Alexandra Post Office
SINGAPORE, 9115
6th Floor, Inchcape House
450-452 Alexandra Road
SINGAPORE 0511
Tel: 631788
Telex: HPSGSO RS 34209
Cable: HEWPACK, Singapore
A,CH,CS,E,MS,P

Dynamar International Ltd.
Unit 05-11 Block 6
Kolam Ayer Industrial Estate
***SINGAPORE** 1334*
Tel: 747-6188
Telex: RS 26283
CM

SOUTH AFRICA

Hewlett-Packard So Africa (Pty.) Ltd.
P.O. Box 120
Howard Place **CAPE PROVINCE** 7450
Pine Park Center, Forest Drive, Pinelands
CAPE PROVINCE 7405
Tel: 53-7954
Telex: 57-20006
A,CH,CM,E,MS,P

Hewlett-Packard So Africa (Pty.) Ltd.
P.O. Box 37099
92 Overport Drive
DURBAN 4067
Tel: 28-4178, 28-4179, 28-4110
Telex: 6-22954
CH,CM

Hewlett-Packard So Africa (Pty.) Ltd.
6 Linton Arcade
511 Cape Road
Linton Grange
PORT ELIZABETH 6001
Tel: 041-302148
CH

Hewlett-Packard So Africa (Pty.) Ltd. P.O.Box 33345
Glenstantia 0010 **TRANSVAAL**
1st Floor East
Constantia Park Ridge Shopping Centre
Constantia Park
PRETORIA
Tel: 982043
Telex: 32163
CH,E

Hewlett-Packard So Africa (Pty.) Ltd.
Private Bag Wendywood
SANDTON 2144
Tel: 802-5111, 802-5125
Telex: 4-20877
Cable: HEWPACK Johannesburg
A,CH,CM,CS,E,MS,P

SPAIN

Hewlett-Packard Española S.A.
Calle Entenza, 321
E-BARCELONA 29
Tel: 322.24.51, 321.73.54
Telex: 52603 hpbee
A,CH,CS,E,MS,P

Hewlett-Packard Española S.A.
Calle San Vicente S/No
Edificio Albia II
E-BILBAO 1
Tel: 423.83.06
A,CH,E,MS

Hewlett-Packard Española S.A.
Crta. de la Coruña, Km. 16, 400
Las Rozas
E-MADRID
Tel: (1) 637.00.11

CH,CS,M

Hewlett-Packard Española S.A.
Avda. S. Francisco Javier, S/no
Planta 10. Edificio Sevilla 2,
E-SEVILLA 5
Tel: 64.44.54
Telex: 72933
A,CS,MS,P

Hewlett-Packard Española S.A.
Calle Ramon Gordillo, 1 (Entlo.3)
E-VALENCIA 10
Tel: 361-1354
CH,P

SWEDEN

Hewlett-Packard Sverige AB
Sunnanvagen 14K
S-22226 **LUND**
Tel: (046) 13-69-79
Telex: (854) 17886 (via Spånga office)
CH

Hewlett-Packard Sverige AB
Vastra Vintergatan 9
S-70344 **OREBRO**
Tel: (19) 10-48-80
Telex: (854) 17886 (via Spånga office)
CH

Hewlett-Packard Sverige AB
Skalholtsgatan 9, Kista
Box 19
S-16393 **SPÅNGA**
Tel: (08) 750-2000
Telex: (854) 17886
A,CH,CM,CS,E,MS,P

Hewlett-Packard Sverige AB
Frötallisgatan 30
S-42132 **VÄSTRA-FRÖLUNDA**
Tel: (031) 49-09-50
Telex: (854) 17886 (via Spånga office)
CH,E,P

SWITZERLAND

Hewlett-Packard (Schweiz) AG
Clarastrasse 12
CH-4058 **BASLE**
Tel: (61) 33-59-20
A

Hewlett-Packard (Schweiz) AG
7, rue du Bois-du-Lan
Case Postale 365
CH-1217 **MEYRIN** 1
Tel: (0041) 22-83-11-11
Telex:27333 HPAG CH
CH,CM,CS

Hewlett-Packard (Schweiz) AG
Allmend 2
CH-8967 **WIDEN**
Tel: (0041) 57 31 21 11
Telex: 53933 hpag ch
Cable: HPAG CH
A,CH,CM,CS,E,MS,P

SYRIA

General Electronic Inc.
Nuri Basha P.O. Box 5781
DAMASCUS
Tel: 33-24-87
Telex: 11216 ITIKAL SY
Cable: ELECTROBOR DAMASCUS
E

Middle East Electronics
Place Azmé
P.O.Box 2308
DAMASCUS
Tel: 334592
Telex: 11304 SATACO SY
M,P

TAIWAN

Hewlett-Packard Far East Ltd.
Kaohsiung Office
2/F 68-2, Chung Cheng 3rd Road
KAOHSIUNG
Tel: 241-2318, 261-3253
CH,CS,E

Hewlett-Packard Far East Ltd.
Taiwan Branch
5th Floor
205 Tun Hwa North Road
TAIPEI
Tel: (02) 712-0404
Cable:HEWPACK Taipei
A,CH,CM,CS,E,M,P

Ing Lih Trading Co.
3rd Floor, 7 Jen-Ai Road, Sec. 2
TAIPEI 100
Tel: (02) 3948191
Cable: INGLIH TAIPEI
A

THAILAND

Unimesa
30 Patpong Ave., Suriwong
***BANGKOK** 5*
Tel: 235-5727
Telex: 84439 Simonco TH
Cable: UNIMESA Bangkok
A,CH,CS,E,M

Bangkok Business Equipment Ltd.
5/5-6 Dejo Road
BANGKOK
Tel: 234-8670, 234-8671
Telex: 87669-BEQUIPT TH
Cable: BUSIQUIPT Bangkok
P

TRINIDAD & TOBAGO

Caribbean Telecoms Ltd.
50/A Jerningham Avenue
P.O. Box 732
PORT-OF-SPAIN
Tel: 62-44213, 62-44214
Telex: 235,272 HUGCO WG
CM,E,M,P

TUNISIA

Tunisie Electronique
31 Avenue de la Liberte
TUNIS
Tel: 280-144
E,P

Corema
1 ter. Av. de Carthage
TUNIS
Tel: 253-821
Telex: 12319 CABAM TN
M

TURKEY

Teknim Company Ltd.
Iran Caddesi No. 7
*Kavaklidere, **ANKARA***
Tel: 275800
Telex: 42155 TKNM TR
E

E.M.A.
Medina Eldem Sokak No.41/6
Yuksel Caddesi
ANKARA
Tel: 175 622
M

UNITED ARAB EMIRATES

Emitac Ltd.
P.O. Box 1641
SHARJAH
Tel: 354121, 354123
Telex: 68136 Emitac Sh
CH,CS,E,M,P

UNITED KINGDOM

GREAT BRITAIN

Hewlett-Packard Ltd.
Trafalgar House
Navigation Road
ALTRINCHAM
Chesire WA14 1NU
Tel: (061) 928-6422
Telex: 668068
A,CH,CS,E,M

Hewlett-Packard Ltd.
Oakfield House, Oakfield Grove
Clifton
BRISTOL BS8 2BN, Avon
Tel: (027) 38606
Telex: 444302
CH,M,P

SALES & SUPPORT OFFICES

Arranged alphabetically by country

GREAT BRITAIN (Cont'd)

Hewlett-Packard Ltd.
Fourier House
257-263 High Street
LONDON COLNEY
Herts., AL2 1HA, St. Albans
Tel: (0727) 24400
Telex: 1-8952716
CH,CS,E

Hewlett-Packard Ltd.
Quadrangle
106-118 Station Road
REDHILL, Surrey
Tel: (0737) 68655
Telex: 947234
CH,CS,E

Hewlett-Packard Ltd.
Avon House
435 Stratford Road
SHIRLEY, Solihull
West Midlands B90 4BL
Tel: (021) 745 8800
Telex: 339105
CH

Hewlett-Packard Ltd.
West End House 41
High Street, West End
SOUTHAMPTON
Hampshire S03 3DQ
Tel: (703) 886767
Telex: 477138
CH

Hewlett-Packard Ltd.
King Street Lane
WINNERSH, Wokingham
Berkshire RG11 5AR
Tel: (0734) 784774
Telex: 847178
A,CH,E,M

Hewlett-Packard Ltd.
Nine Mile Ride
WOKINGHAM
Berkshire, 3RG11 3LL
Tel: 3446 3100
Telex: 84-88-05
CH,CS,E

NORTHERN IRELAND

Cardiac Services Company
95A Finaghy Road South
***BELFAST** BT 10 0BY*
Tel: (0232) 625-566
Telex: 747626
M

SCOTLAND

Hewlett-Packard Ltd.
SOUTH QUEENSFERRY
West Lothian, EH30 9GT
Tel: (031) 3311188
Telex: 72682
A,CH,CM,CS,E,M

UNITED STATES

Alabama

Hewlett-Packard Co.
P.O. Box 7000
8290 Whitesburg Drive, S.E.
HUNTSVILLE, AL 35802
Tel: (205) 830-2000
CH,CM,CS,E,M*

Arizona

Hewlett-Packard Co.
8080 Point Parkway West
PHOENIX, AZ 85044
Tel: (602) 273-8000
A,CH,CM,CS,E,MS

Hewlett-Packard Co.
2424 East Aragon Road
TUCSON, AZ 85706
Tel: (602) 889-4631
CH,E,MS**

California

Hewlett-Packard Co.
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4BRISBANE, CA 94005
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Hewlett-Packard Co.
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Tel: (213) 702-8363
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Hewlett-Packard Co.
P.O. Box 7830 (93747)
5060 E. Clinton Avenue, Suite 102
FRESNO, CA 93727
Tel: (209) 252-9652
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Hewlett-Packard Co.
P.O. Box 4230
1430 East Orangethorpe
FULLERTON, CA 92631
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Hewlett-Packard Co.
320 S. Kellogg, Suite B
GOLETA, CA 93117
Tel: (805) 967-3405
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Hewlett-Packard Co.
5400 W. Rosecrans Boulevard
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P.O. Box 92105
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Tel: (213) 970-7500
Telex: 910-325-6608
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Hewlett-Packard Co.
3200 Hillview Avenue
PALO ALTO, CA 94304
Tel: (415) 857-8000
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Hewlett-Packard Co.
P.O. Box 15976 (95813)
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SACRAMENTO, CA 95834
Tel: (916) 929-7222
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Hewlett-Packard Co.
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Hewlett-Packard Co.
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Hewlett-Packard Co.
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47 Barnes Industrial Road South
P.O. Box 5007
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Florida

Hewlett-Packard Co.
P.O. Box 24210 (33307)
2901 N.W. 62nd Street
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Hewlett-Packard Co.
P.O. Box 13910
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ORLANDO, FL 32809
Tel: (305) 859-2900
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Hewlett-Packard Co.
5750B N. Hoover Blvd., Suite 123
TAMPA, FL 33614
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P.O. Box 105005
30348 **ATLANTA**,GA
2000 South Park Place
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Tel: (404) 955-1500
Telex: 810-766-4890
A,CH,CM,CS,E,MP

Hawaii

Hewlett-Packard Co.
Kawaiahao Plaza, Suite 190
567 South King Street
HONOLULU, HI 96813
Tel: (808) 526-1555
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Illinois

Hewlett-Packard Co.
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304 Eldorado Road
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Hewlett-Packard Co.
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DOWNERS GROVE, IL 60515
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P.O. Box 50807
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Suite 203
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10300 Linn Station Road
Suite 100
LOUISVILLE, KY 40223
Tel: (502) 426-0100
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Louisiana

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P.O. Box 1449
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160 James Drive East
ST. ROSE, LA 70087
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Maryland

Hewlett-Packard Co.
3701 Koppers Street
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Tel: (301) 644-5800
Telex: 710-862-1943
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Hewlett-Packard Co.
2 Choke Cherry Road
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Tel: (301) 948-6370
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Tel: (617) 861-8960
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Hewlett-Packard Co.
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Tel: (313) 476-6400
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Minnesota

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Nebraska

Hewlett-Packard
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OMAHA, NE 68154
Tel: (402) 334-1813
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P.O. Box 11634 (87192)
11300 Lomas Blvd.,N.E.
ALBUQUERQUE, NM 87112
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WOODBURY, NY 11797
Tel: (516) 921-0300
Telex: 510-221-2183
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6

SALES & SUPPORT OFFICES

Arranged alphabetically by country

UNITED STATES (Cont'd)

North Carolina
Hewlett-Packard Co.
P.O. Box 26500 (27420)
5605 Roanne Way
GREENSBORO, NC 27409
Tel: (919) 852-1800
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Ohio
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9920 Carver Road
CINCINNATI, OH 45242
Tel: (513) 891-9870
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Hewlett-Packard Co.
16500 Sprague Road
CLEVELAND, OH 44130
Tel: (216) 243-7300
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Hewlett-Packard Co.
962 Crupper Ave.
COLUMBUS, OH 43229
Tel: (614) 436-1041
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Hewlett-Packard Co.
P.O. Box 280
330 Progress Rd.
DAYTON, OH 45449
Tel: (513) 859-8202
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Oklahoma
Hewlett-Packard Co.
P.O. Box 75609 (73147)
304 N. Meridian, Suite A
3
OKLAHOMA CITY, OK 73107
Tel: (405) 946-9499
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Hewlett-Packard Co.
3840 S. 103rd E. Avenue
Logan Building, Suite 100
TULSA, OK 74145
Tel: (918) 665-3300
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Oregon
Hewlett-Packard Co.
9255 S. W. Pioneer Court
WILSONVILLE, OR 97070
Tel: (503) 682-8000
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Pennsylvania
Hewlett-Packard Co.
1021 8th Avenue
KING OF PRUSSIA, PA 19046
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Hewlett-Packard Co.
111 Zeta Drive
PITTSBURGH, PA 15238
Tel: (412) 782-0400
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South Carolina
Hewlett-Packard Co.
P.O. Box 21708 (29221)
Brookside Park, Suite 122
1 Harbison Way
COLUMBIA, SC 29210
Tel: (803) 732-0400
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Tennessee
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3070 Directors Row
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Texas
Hewlett-Packard Co.
Suite C-110
4171 North Mesa
EL PASO, TX 79902
Tel: (915) 533-3555
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Hewlett-Packard Co.
P.O. Box 42816 (77042)
10535 Harwin Street
HOUSTON, TX 77036
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Hewlett-Packard Co.
P.O. Box 1270
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RICHARDSON, TX 75080
Tel: (214) 231-6101
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1020 Central Parkway South
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Tel: (512) 494-9336
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3530 W. 2100 South
SALT LAKE CITY, UT 84119
Tel: (801) 974-1700
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Hewlett-Packard Co.
P.O. Box 9669 (23228)
RICHMOND, Va. 23228
4305 Cox Road
GLEN ALLEN, Va. 23060
Tel: (804) 747-7750
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Washington
Hewlett-Packard Co.
15815 S.E. 37th Street
BELLEVUE, WA 98006
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Hewlett-Packard Co.
Suite A
708 North Argonne Road
SPOKANE, WA 99206
Tel: (509) 922-7000
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Hewlett-Packard Co.
P.O. Box 4297
4604 MacCorkle Ave., S.E.
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Wisconsin
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150 S. Sunny Slope Road
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URUGUAY

Pablo Ferrando S.A.C. e I.
Avenida Italia 2877
Casilla de Correo 370
MONTEVIDEO
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VENEZUELA

Hewlett-Packard de Venezuela C.A.
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CARACAS 1071
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C,E*

Hewlett-Packard de Venezuela C.A.
Calle Vargas Rondon
Edificio Seguros Carabobo, Piso 10
VALENCIA
Tel:(041) 51 385
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Colimodio S.A.
Este 2 - Sur 21 No. 148
Apartado 1053
***CARACAS** 1010*
Tel: 571-3511
Telex: 21529 COLMODIO
M

ZIMBABWE

Field Technical Sales
45 Kelvin Road, North
P.B. 3458
SALISBURY
Tel: 705 231
Telex: 4-122 RH
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HEADQUARTERS OFFICES

If there is no sales office listed for your area, contact one of these headquarters offices.

NORTH/CENTRAL AFRICA

Hewlett-Packard S.A.
7 Rue du Bois-du-Lan
CH-1217 **MEYRIN** 1, Switzerland
Tel: (022) 83 12 12
Telex: 27835 hpse
Cable: HEWPACKSA Geneve

ASIA

Hewlett-Packard Asia Ltd.
6th Floor, Sun Hung Kai Centre
30 Harbour Rd.
G.P.O. Box 795
HONG KONG
Tel: 5-832 3211
Telex: 66678 HEWPA HX
Cable: HEWPACK HONG KONG

CANADA

Hewlett-Packard (Canada) Ltd.
6877 Goreway Drive
MISSISSAUGA, Ontario L4V 1M8
Tel: (416) 678-9430
Telex: 610-492-4246

EASTERN EUROPE

Hewlett-Packard Ges.m.b.h.
Lieblgasse 1
P.O.Box 72
A-1222 **VIENNA**, Austria
Tel: (222) 2365110
Telex: 1 3 4425 HEPA A

NORTHERN EUROPE

Hewlett-Packard S.A.
Uilenstede 475
NL-1183 AG **AMSTELVEEN**
The Netherlands
P.O.Box 999
NL-1180 AZ **AMSTELVEEN**
The Netherlands
Tel: 20 437771

OTHER EUROPE

Hewlett-Packard S.A.
7 rue du Bois-du-Lan
CH-1217 **MEYRIN 1**, Switzerland
Tel: (022) 83 1212
Telex: 27835 hpse
Cable: HEWPACKSA Geneve

MEDITERRANEAN AND MIDDLE EAST

Hewlett-Packard S.A.
Mediterranean and Middle East
Operations
Atrina Centre
32 Kifissias Ave.
Maroussi, **ATHENS**, Greece
Tel: 682 88 11
Telex: 21-6588 HPAT GR
Cable: HEWPACKSA Athens

EASTERN USA

Hewlett-Packard Co.
4 Choke Cherry Road
Rockville, MD 20850
Tel: (301) 258-2000

MIDWESTERN USA

Hewlett-Packard Co.
5201 Tollview Drive
ROLLING MEADOWS, IL 60008
Tel: (312) 255-9800

SOUTHERN USA

Hewlett-Packard Co.
P.O. Box 105005
450 Interstate N. Parkway
ATLANTA, GA 30339
Tel: (404) 955-1500

WESTERN USA

Hewlett-Packard Co.
3939 Lankershim Blvd.
LOS ANGELES, CA 91604
Tel: (213) 877-1282

OTHER INTERNATIONAL AREAS

Hewlett-Packard Co.
Intercontinental Headquarters
3495 Deer Creek Road
PALO ALTO, CA 94304
Tel: (415) 857-1501
Telex: 034-8300
Cable: HEWPACK

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